Digital Teknik II / Digital Design II

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Digital Teknik / Digital Design

Modul 4

Shift Registers

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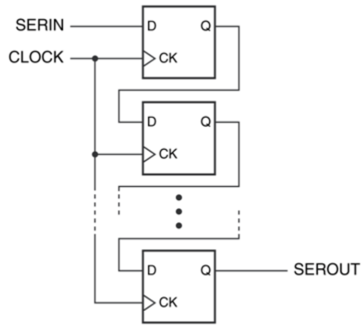
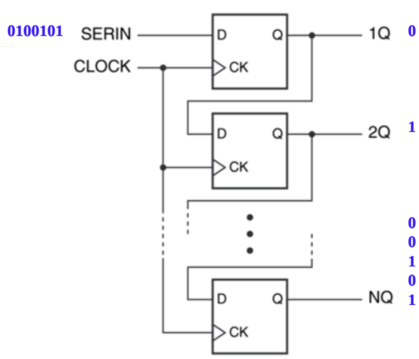
Serial in Serial out Shift Register



Structure of a serial-in, serial-out shift register.

A shift register shifts its stored data by one bit position at each tick of the clock. If there are n flip flops then the first bit given at SERIN will appear at SEROUT after n clock ticks.
This is a serial in serial out shift register. This type of shift register can be used to delay a signal by n counts.

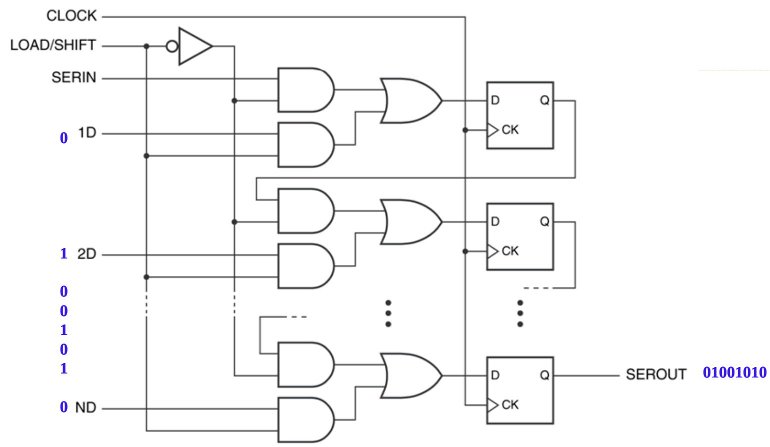
Serial in Parallel out Shift Register



Structure of a serial-in, parallel-out shift register.

Data is shifted one position at each tick of the clock

Parallel in Serial out shift Register



Structure of a parallel-in, serial-out shift register.

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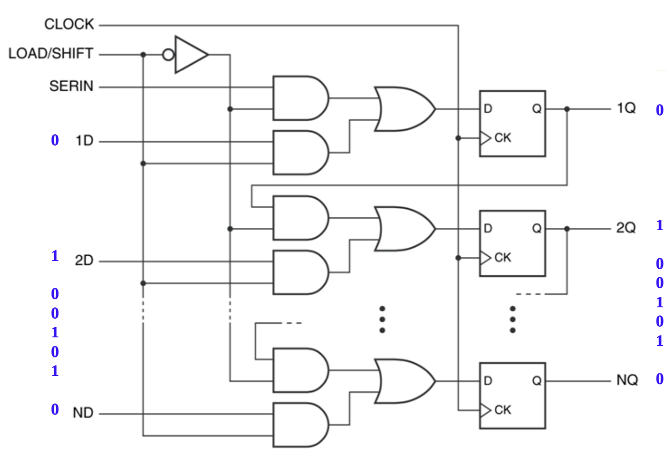
Parallel in Parallel out Register



Structure of a parallel-in, parallel-out shift register.

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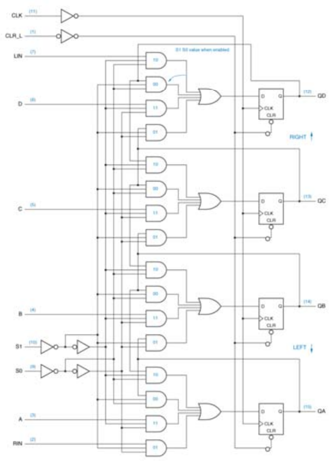
74194 4 Bit Universal Bidirectional Register



Why 2^{12} possible combinations ?

There are 2^{12} possible combinations of current state and input. LIN is input for left shift where as RIN is input for right shift. It is also called universal shift register as it can be made to use what ever way we like or desire, it can shift data in both direction left or right using RIN & LIN.

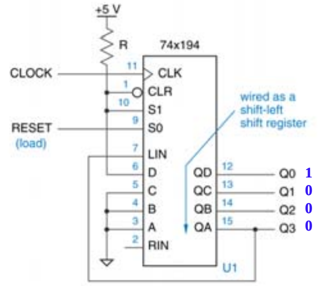
Function Table for 74194 Shift Register

Function	Inputs S1	Inputs S0	Next state QA*	Next state QB*	Next state QC*	Next state QD*
Hold	0	0	QA	QB	QC	QD
Shift right	0	1	RIN	QA	QB	QC
Shift left	1	0	QB	QC	QD	LIN
Load	1	1	A	B	C	D

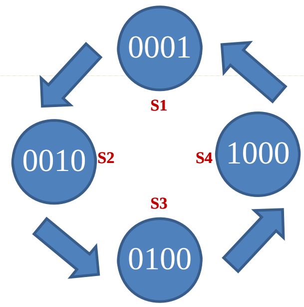
Function table for the 74×194 4-bit universal shift register.

These registers are seldom used these days because they are typically build in PLD and FPGA, earlier shown registers are all unidirectional as the data only flows in one direction, 74194 is bidirectional shift register by using the **Shift right or Shift Left** control inputs. It is highly condensed function table.

Shift Register Counter



Simplest design for a 4-bit, 4-state ring counter with a single circulating 1.



Serial or Parallel conversion is a "data" application however, they can be used as non-data application. Typically, a shift register can be combined with combinational logic to form a state machine whose state diagram is cyclic, it is called shift-register counter. This is constructed as a ring counter which provides 4 different states, once RESET is asserted the circuit loads 0001 and after RESET is un-asserted with each clock tick the counter moves from **0001 – 0010 – 0100 – 1000 and as QA is connected to LIN so it will repeat the sequence**.

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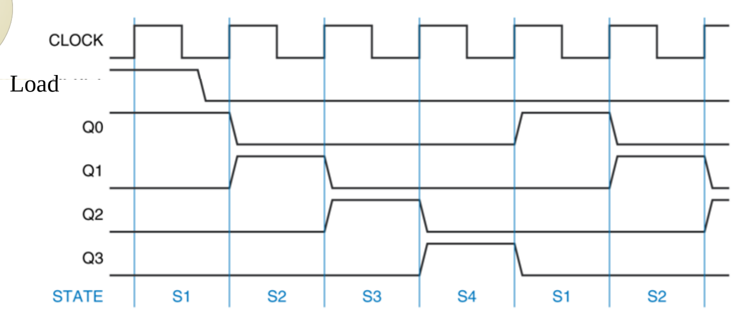
Timing Diagram 4 bit Ring Counter



Timing diagram for a 4-bit ring counter.

Ring counter has one **major issue,** if by chance any bit is changed due to some reason it will behave inconsistently and will move in undesired states. For example due to a hardware problem (S1=0000), then it will remain in that state for ever.

In general an **n bit** ring counter visits **n states** in a cycle.

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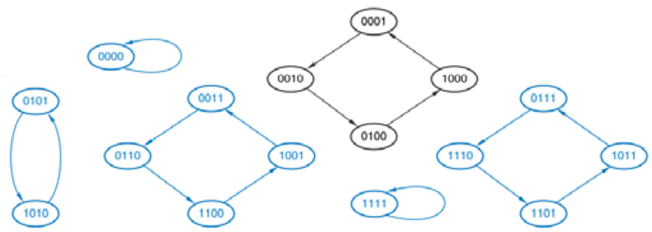
Undesirable States



State diagram for a simple ring counter.

The counter has 4 output so the possible states are 16, we can see that there are 12 states which are undesirable states, so one has to avoid that system should not go into these and may have to design with a **minimal risk** approach so that the system goes to a **”safe” state**.

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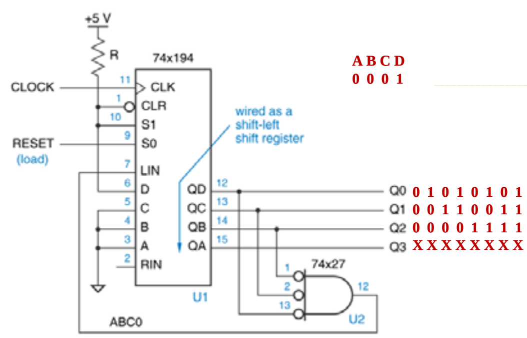
Self Correcting Design



Self-correcting 4-bit, 4-state ring counter with a single circulating 1.

Self correcting design will lead all undesired states to normal desired states.

For an n bit ring counter, correction can be achieved within (n – 1) clock ticks. Here we are using 3 input NOR gate to self correct the abnormality.

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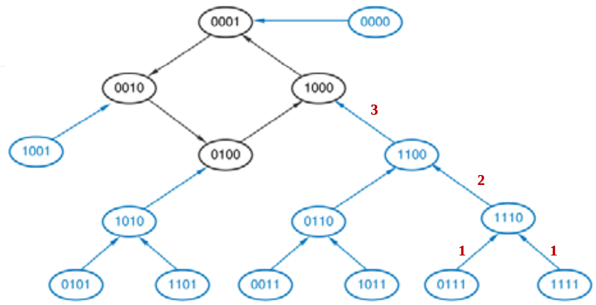
Self Correcting State Diagram



State diagram for a self-correcting ring counter.

It can be seen from the diagram that no mater what state you start in after 3 clock ticks you will end up into the normal state.

This also means that RESET is not necessary for such a circuit, however typically RESET is part of the circuit as the ring counter can start at the same state with all other circuit in the system.

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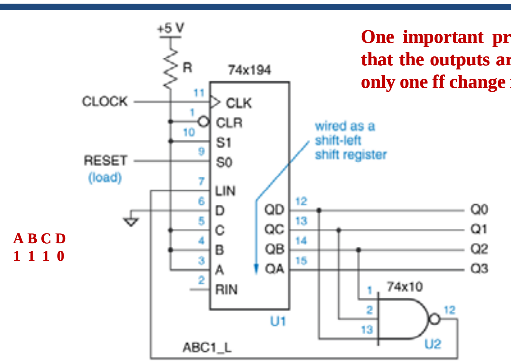
Self Correcting RC with a Single Circulating 0

One important property of ring counters is that the outputs are glitch free due to exactly only one ff change its output in each state.



Self-correcting 4-bit, 4-state ring counter with a single circulating 0.

NOR gates are more difficult to construct than the NAND gates in CMOS/TTL, so we change the circuit with a NAND gate and we also pull down D input and pull up A, B and C to have a single circulating 0.

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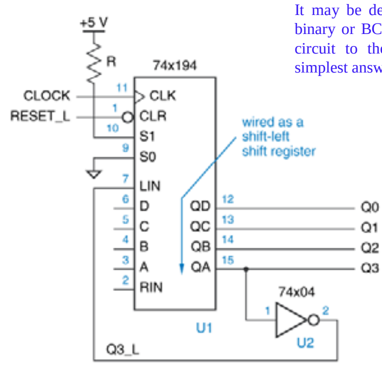
Johnson Counter

It may be desired to provides individual digit outputs rather than a binary or BCD output. Which can be achieved by adding a decoder circuit to the binary counter. Fortunately, Johnson counter is the simplest answer to this problem.



Basic 4-bit, 8-state Johnson counter.

If the complemented serial output is fed back to the ring counter it becomes a Johnson counter and will have **2n states**. It is also named as ”Twisted Ring” or ”Moebius”

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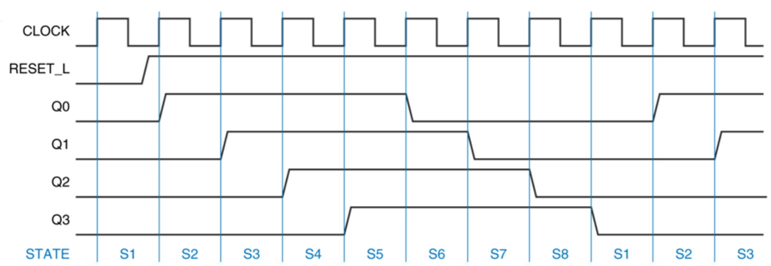
Timing Diagram



Timing diagram for a 4-bit Johnson counter.

Note an important property of this counter ?

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States of Johnson Counter

State Name	Q3	Q2	Q1	Q0
S1	0	0	0	0
S2	0	0	0	1
S3	0	0	1	1
S4	0	1	1	1
S5	1	1	1	1
S6	1	1	1	0
S7	1	1	0	0
S8	1	0	0	0

States of a 4-bit Johnson counter.

Johnson counter also suffers the same problem of undesirable states occurrence which for an n bit Johnson counter are $2^n - 2n$.

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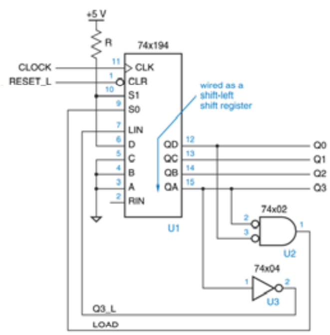
Self Correction for 4 bit Johnson Counter



Self-correcting 4-bit, 8-state Johnson counter.

State Name	Q3	Q2	Q1	Q0	Decoding
S1	0	0	0	0	Q3′ · Q0′
S2	0	0	0	1	Q1′ · Q0
S3	0	0	1	1	Q2′ · Q1
S4	0	1	1	1	Q3′ · Q2
S5	1	1	1	1	Q3 · Q0
S6	1	1	1	0	Q1 · Q0′
S7	1	1	0	0	Q2 · Q1′
S8	1	0	0	0	Q3 · Q2′

States of a 4-bit Johnson counter.

The total number of abnormal (undesired) states are = $2^n - 2n = 16 - 8 = 8$. This circuit loads 0001 when ever the current state is 0xx0.

Self correction in Johnson counter is within n – 2 ticks (compared to n – 1 of the ring counter).

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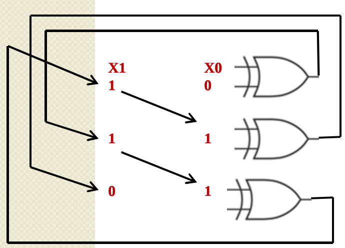
Linear Feedback Shift-Register

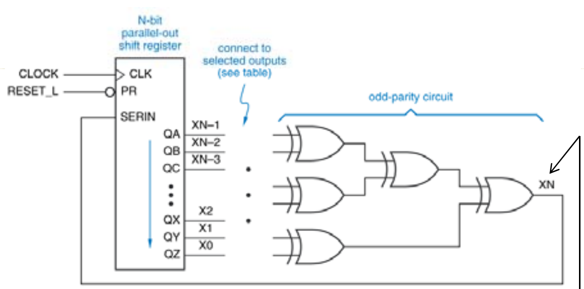
The problem with standard shift register counter is that it has far less normal states, so a linear feedback shift register has **2^n – 1 states**, almost maximum.

It is also called maximum length sequence generator.

It is based on a finite field theory, which says that for any value of n, there exist at least one feedback equation that makes the counter go through all nonzero 2^n – 1 states before repeating.

Linear Feedback Shift-Register





General structure of a linear feedback shift-register counter.

The shift register is preset to 1 0 at the start, now take the example of n = 2, so total states should be 4 – 1 = 3, now using the exclusive OR gate it can be seen that the system goes (sequence through) to the following states: 1 0, 1 1, 0 1 and repeat again.

So the equation X2 = X1 ⊕ X0.

Feedback Equations

n	*Feedback Equation*
2	X2 = X1 ⊕ X0
3	X3 = X1 ⊕ X0
4	X4 = X1 ⊕ X0
5	X5 = X2 ⊕ X0
6	X6 = X1 ⊕ X0
7	X7 = X3 ⊕ X0
8	X8 = X4 ⊕ X3 ⊕ X2 ⊕ X0
12	X12 = X6 ⊕ X4 ⊕ X1 ⊕ X0
16	X16 = X5 ⊕ X4 ⊕ X3 ⊕ X0
20	X20 = X3 ⊕ X0
24	X24 = X7 ⊕ X2 ⊕ X1 ⊕ X0
28	X28 = X3 ⊕ X0
32	X32 = X22 ⊕ X2 ⊕ X1 ⊕ X0

Feedback equations for linear feedback shift-register counters.

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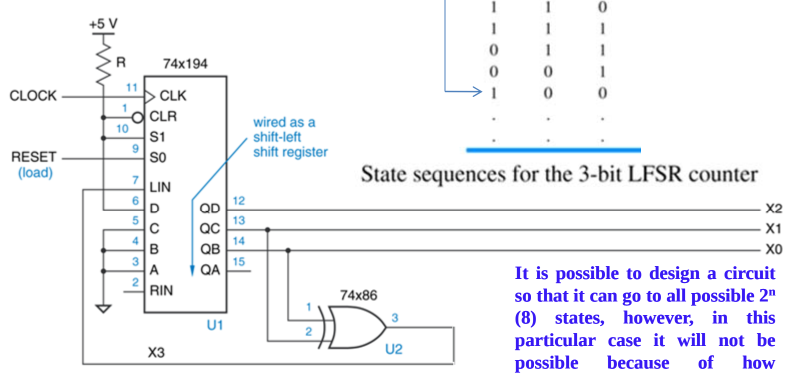
3 Bit LFSR Counter

The counter cycle through 7 states before returning to the starting state.

X2	*X1*	*X0*
1	0	0
0	1	0
1	0	1
1	1	0
1	1	1
0	1	1
0	0	1
1	0	0
.	.	.
.	.	.

State sequences for the 3-bit LFSR counter



It is possible to design a circuit so that it can go to all possible 2^n (8) states, however, in this particular case it will not be possible because of how connections are made, also next state for all zero's will be zero's.

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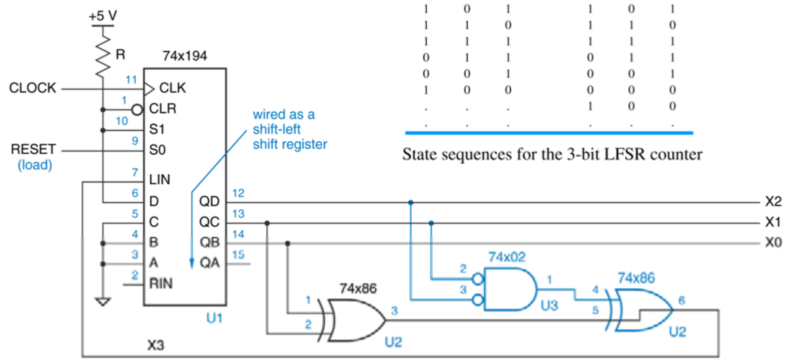
Modified 3 Bit LFSR Counter

This modified circuit can cycle through all possible 2^n states.

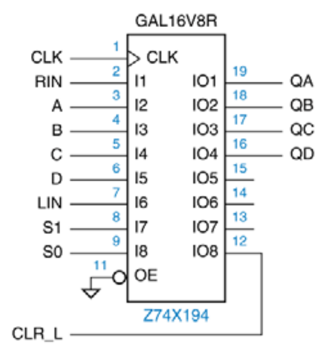
Original Sequence			Modified Sequence		
X2	X1	X0	X2	X1	X0
1	0	0	1	0	0
0	1	0	0	1	0
1	0	1	1	0	1
1	1	0	1	1	0
1	1	1	1	1	1
0	1	1	0	1	1
0	0	1	0	0	1
1	0	0	0	0	0
.	.	.	1	0	0
.	.	.	.	.	.

State sequences for the 3-bit LFSR counter



A 3-bit LFSR counter; modifications to include the all-0s state are shown in color.

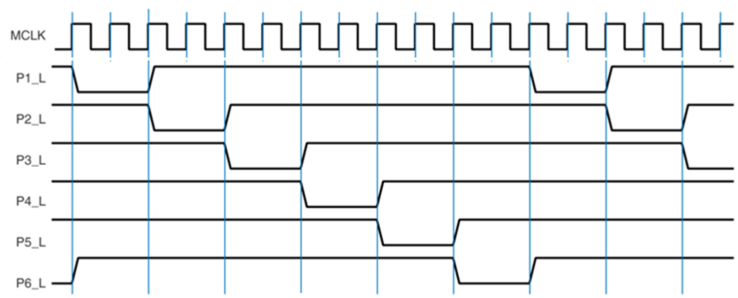
PLD Realization of 74194



PLD realizations of a 74×194-like universal shift register with synchronous clear.

The circuit shown is a realization of 74194 the only difference is that its CLR_L is synchronous where as in the original it is asynchronous.

Example 1



Six-phase timing waveforms required in a certain digital system.

We can see that each phase (Pi_L) last for 2 ticks of the clock, this can be easily constructed using a ring counter.

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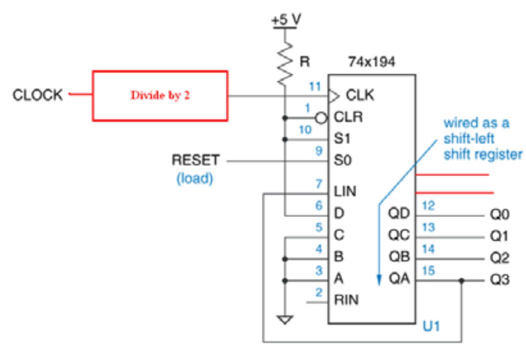
Example 1 possible diagram



It is possible by inserting an extra flip flop to count the 2 ticks of each phase.

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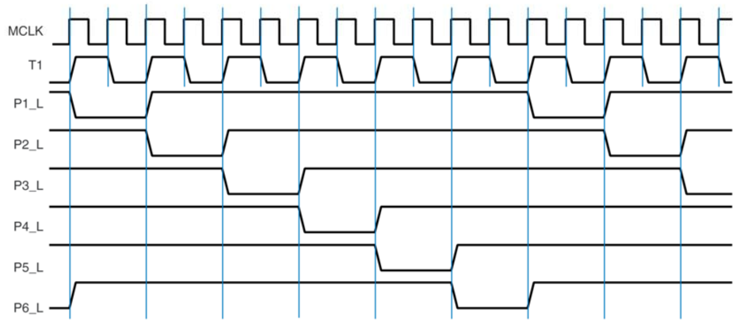
Example 1 Timing Diagram



Six-phase timing waveforms required in a certain digital system.

The input clock MCLK is divided by 2 through a FF so producing the output after every 2 clock cycle.

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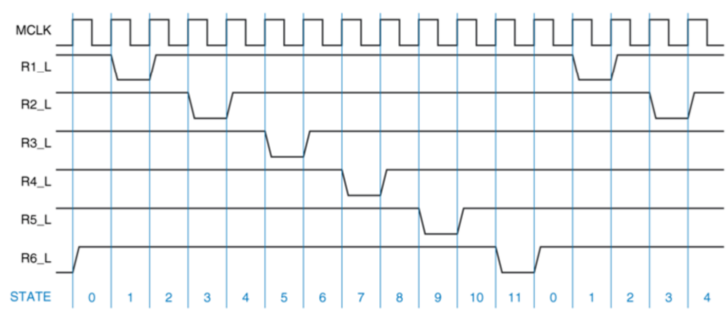
How can we design such system that produce the following waveform



Modified timing waveforms for a digital system.

This is also similar meaning the output is produced after every 2 clock, difference is that output remains in that state for only one clock period and is shifted by one clock time period, what kind of ring counter can produce such an outputs ?

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Function Table

Function	Inputs S2	S1	S0	Next state Q7*	Q6*	Q5*	Q4*	Q3*	Q2*	Q1*	Q0*
Hold	0	0	0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
Load	0	0	1	D7	D6	D5	D4	D3	D2	D1	D0
Shift right	0	1	0	RIN	Q7	Q6	Q5	Q4	Q3	Q2	Q1
Shift left	0	1	1	Q6	Q5	Q4	Q3	Q2	Q1	Q0	LIN
Shift circular right	1	0	0	Q0	Q7	Q6	Q5	Q4	Q3	Q2	Q1
Shift circular left	1	0	1	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Q7
Shift arithmetic right	1	1	0	Q7	Q7	Q6	Q5	Q4	Q3	Q2	Q1
Shift arithmetic left	1	1	1	Q6	Q5	Q4	Q3	Q2	Q1	Q0	0

Function table for an extended-function 8-bit shift register.

This function table give us a behavioural description of a shift register, in addition to load, hold and shift function it can do arithmetic functions as well. Shift left is different than shift right as in SL right input is 0 and for SR we replicate sign bit.

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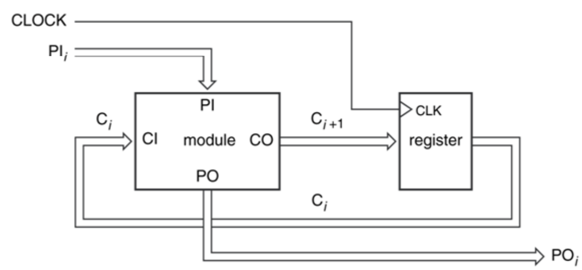
Iterative Circuit



General structure of the sequential-circuit version of an iterative circuit.

An iterative circuit is a combinational circuit so all its primary and boundary inputs must be applied simultaneously, and all its primary and boundary outputs are available after the combinational delay.

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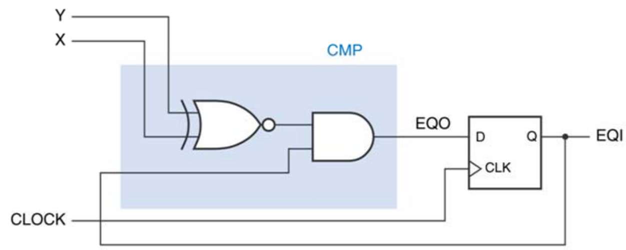
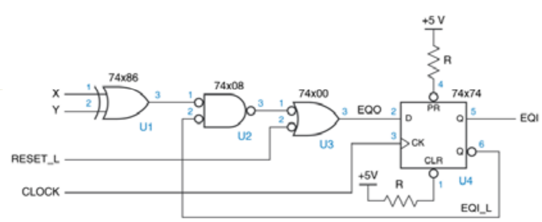
Simplified Serial Comparator Circuit



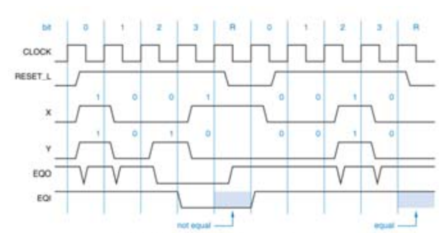
Simplified serial comparator circuit.

Shaded block is the iterative comparator and the flip flop provides the boundary input.

Serial Comparator Circuit

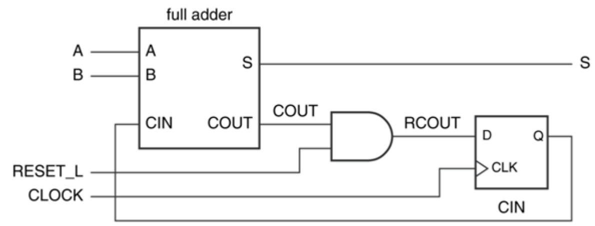


Detailed serial comparator circuit.



Timing diagram for serial comparator circuit.

Serial Binary Adder



Serial binary adder circuit.

Serial Binary adder for any length is shown.

Synchronous System

Most digital systems can be divided into two components:
Control Unit & Data Unit.

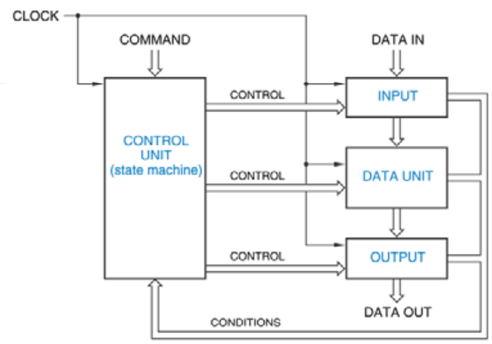
Synchronous systems are simple in design and they are reliable, however, there are certain issues which can result difficulty in achieving reliability.

Control Unit: Responsible for starting and stopping actions in data units, testing various conditions and making decision under various situations.

Data Unit: Storing, Routing and may be combining data.

In general Control Unit is designed as state machines.

Synchronous System



Synchronous system structure.

All flip flops are clocked with the same common clock signal and PRESET/CLEAR inputs are not used. Race and Hazard are not an issue in synchronous system.

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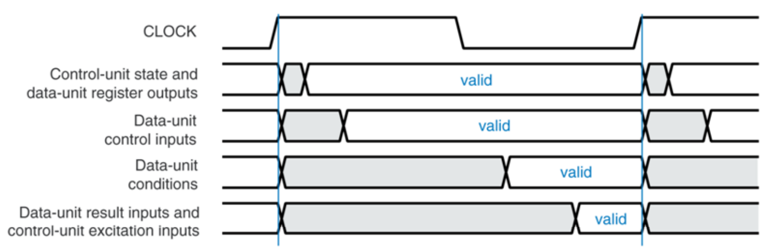
Operation during Single Cycle



Operations during one clock cycle in a synchronous system.

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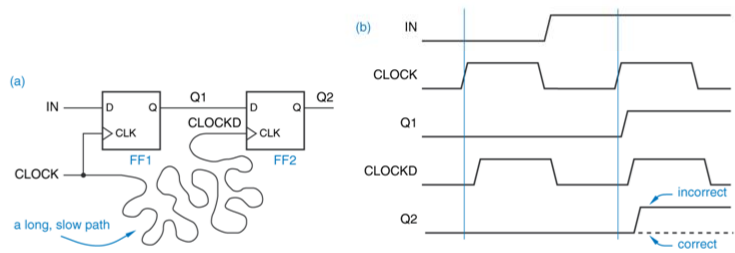
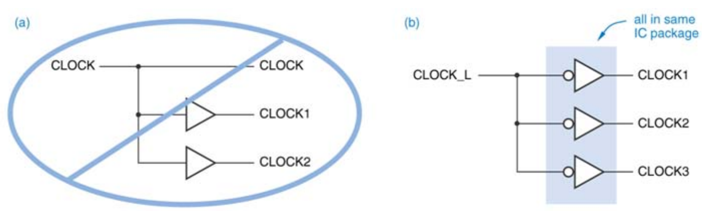
Clock Skew



Clock-skew example.

There are various situations when such a thing happens, for example a long route to reach to FF2 or may be it is routed through a buffer to increase the fan out.

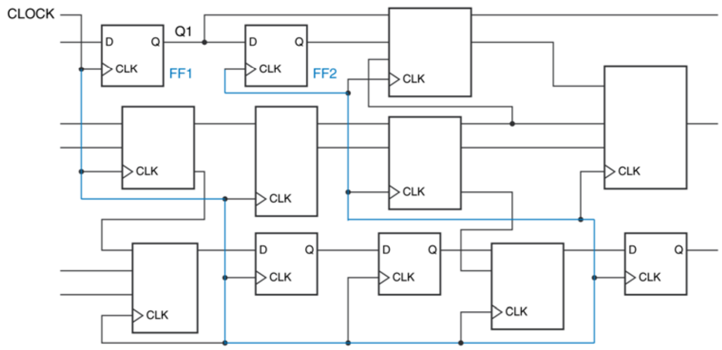
Buffering Clock



Buffering the clock: (a) excessive clock skew; (b) controllable clock skew.

Even in the controllable clock skew problem may not be solved if there is unbalanced load on different buffers, so it is recommended that designer must ensure such balance.

Excessive Skew



A clock-signal path leading to excessive skew.

CAD has routed clock leading to skew problem, also in ASIC design there are different types of wire connections (Polysilicon & Metal), which obviously have different properties so it can also lead to same problem.

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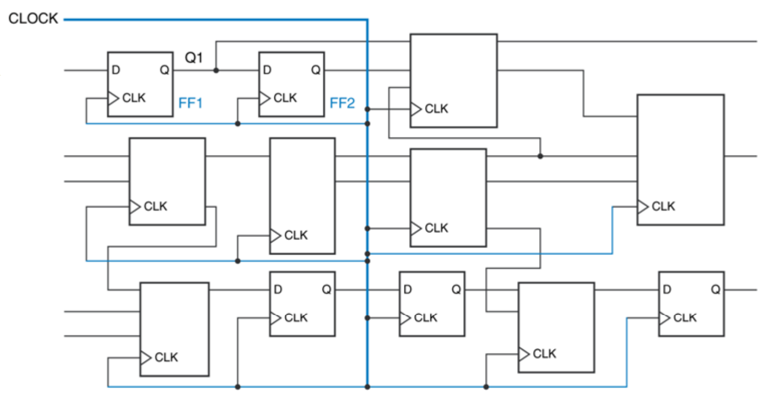
Minimize Skew



Clock-signal routing to minimize skew.

Designer must use fastest type of wire connection for Clock and also use a tree like structure to avoid skew problem.

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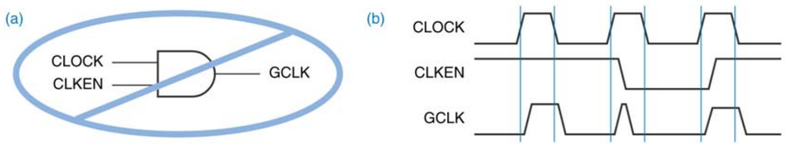
Gating



Bad clock gating: (a) simple-minded circuit; (b) timing diagram.

In some situations a designer may gate the clock with clock enable, which may produce a glitch on GCLK.

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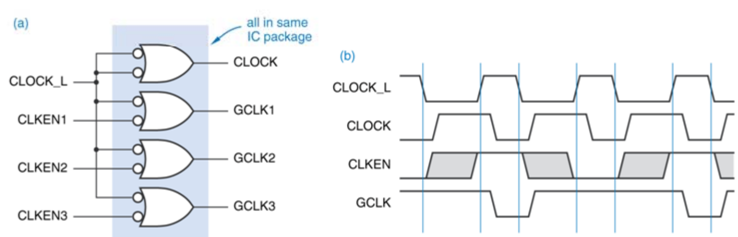
Acceptable Gating



Acceptable clock gating: (a) circuit; (b) timing diagram.

Basically, CLKEN must be stable during the entire duration when CLOCK_L is low.

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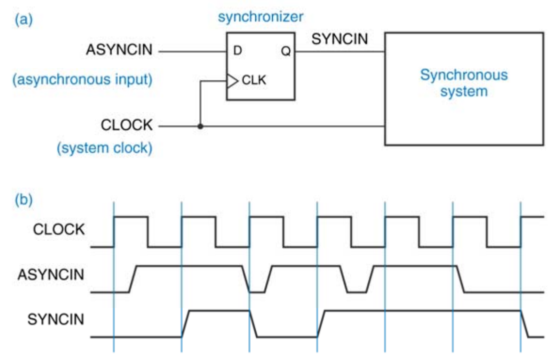
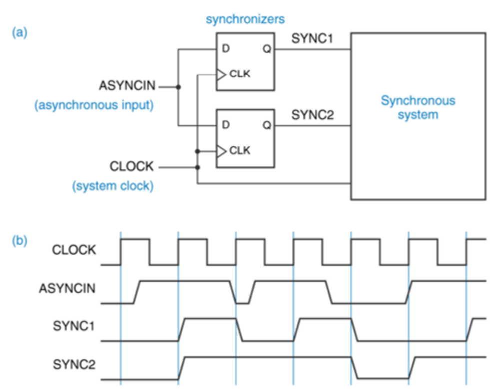
Synchronizer



A single, simple synchronizer: (a) logic diagram; (b) timing.

Theoretically, it is possible to build the entire computer system as a synchronous machine but practically, it is impossible. A simple synchronizer can be build to synch the system with the main synchronous system.

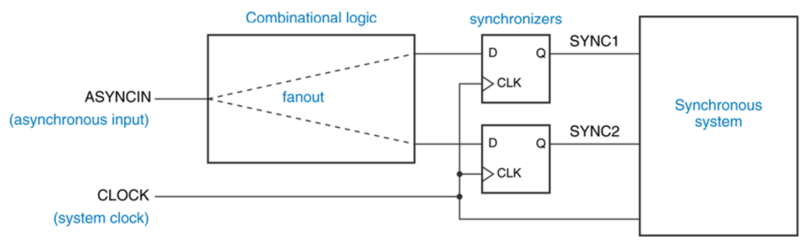
Two Synchronizers for Same Asynchronous Input



Two synchronizers for the same asynchronous input: (a) logic diagram; (b) possible timing.

Due to the reason stated earlier, the synchronizer may not see the ASYNCIN and CLOCK at the same time leading to inconsistent result as shown above.

An Asynchronous Input Driver



An asynchronous input driving two synchronizers through combinational logic.

It may be a combinational circuit as shown above.

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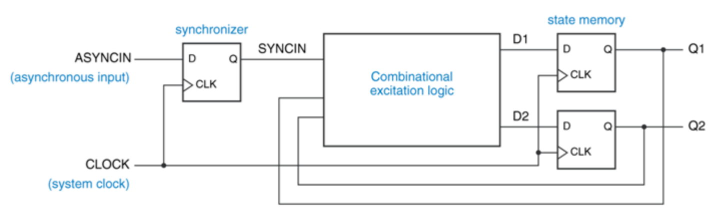
Asynchronous State Machine



An asynchronous state-machine input coupled through a single synchronizer.

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Synchronizer Failure

Metastability occurs when the setup and hold time of a ff is violated.

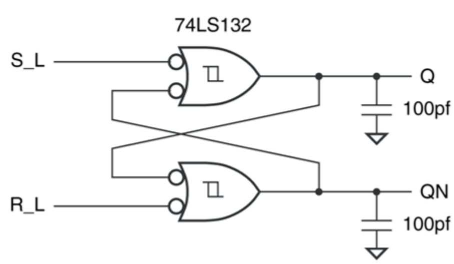
One can force the ff into a valid logic state using input signals that meet the specifications for pulse width, setup time etc.

Second wait so the ff comes out of that meta stable state, question is how long to be waited.

$t_r = t_{clk} - t_{comb} - t_{setup}$

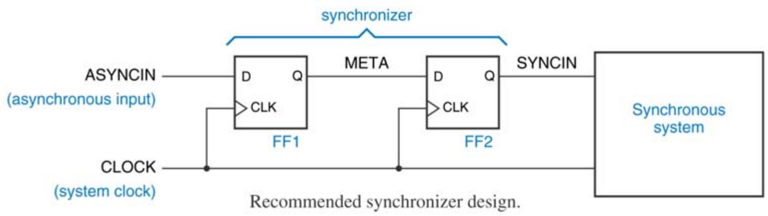
(t_{clk} : Clock period time, t_{comb} : PD time of combinational logic, t_{setup} : Set up time of ffs.

Metastable-Proof



A failed attempt to build a metastable-proof $\bar{S}$-$\bar{R}$flip-flop.

Synchronizer Design



Recommended synchronizer design.

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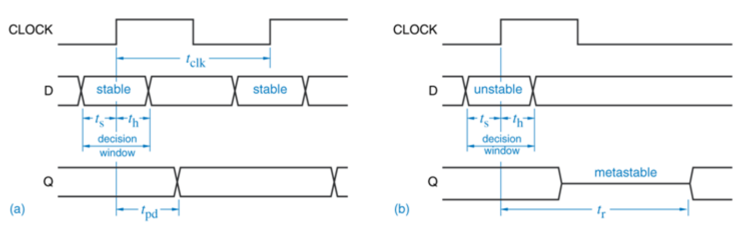
Timing Parameters



Timing parameters for metastability analysis: (a) normal flip-flop operation; (b) metastable behavior.

$t_r = t_{clk} - t_{comb} - t_{setup}$

(t_{clk} : Clock period time, t_{comb} : PD time of combinational logic, t_{setup} : Set up time of ffs.)

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Metastability Parameters

Reference	Device	τ (ns)	T_o (s)	t_r (ns)
Chaney (1983)	74LS74	1.50	4.0 10^{-1}	77.7
Chaney (1983)	74S74	1.70	1.0 10^{-6}	66.1
Chaney (1983)	74F74	0.40	2.0 10^{-4}	17.7
TI (1997)	74LSxx	1.35	4.8 10^{-3}	64.0
TI (1997)	74Sxx	2.80	1.3 10^{-9}	90.3
TI (1997)	74ALSxx	1.00	8.7 10^{-6}	41.1
TI (1997)	74ASxx	0.25	1.4 10^{3}	15.0
TI (1997)	74Fxx	0.11	1.9 10^{8}	7.9
TI (1997)	74HCxx	1.82	1.5 10^{-6}	71.6
TI (1997)	74ACxx	0.36	1.1 10^{-4}	15.7
Cypress (1997)	PALC22V10B-20	0.26	5.6 10^{-11}	7.6*
Cypress (1997)	PALCE22V10-7	0.19	1.3 10^{-13}	4.4*
Xilinx (1997)	7300-series CPLD	0.29	1.0 10^{-15}	5.3*
Xilinx (1997)	9500-series CPLD	0.17	9.6 10^{-18}	2.3*

Metastability parameters for some common devices.

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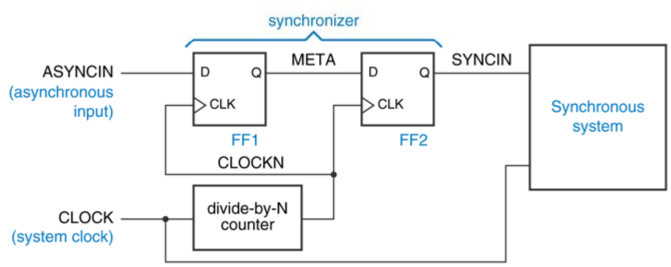
Multiple Cycle Synchronizer



Multiple-cycle synchronizer.

The clock is slowed down, usually division of 2 or 3 gives a good synchronizer.

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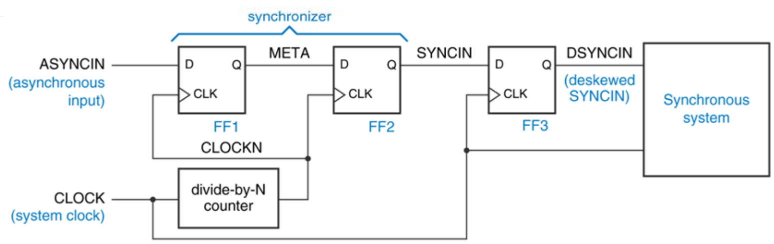
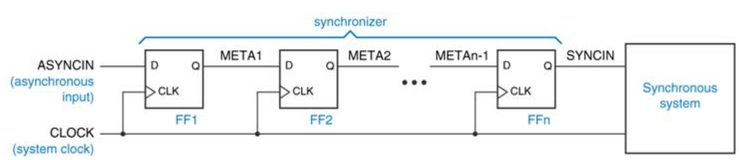
Multiple Cycle Synchronizer with Deskewing



Multiple-cycle synchronizer with deskewing.

There could be similar skew problem for CLOCKN signal so a better option is given above, where it synched with the CLOCK.

Cascaded Synchronizer



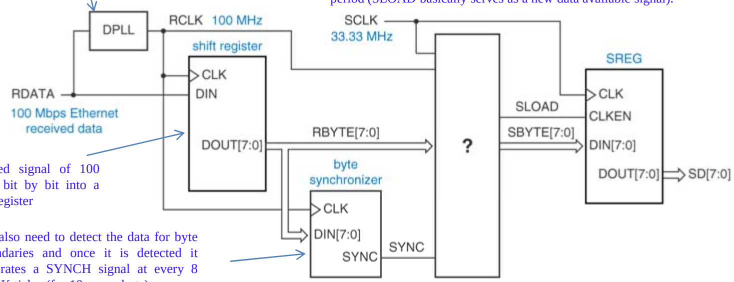
Cascaded synchronizer.

In an n cycle synchronizer, the larger is the value of n longer it takes by the synchronous system to see the change happened in the asynchronous input, this is the price paid by reliable systems.
So rather than dividing, cascading the synchronizers works better.

Ethernet Synchronization

Generates/recovers a 100 MHz signal which is in phase with the input.

As Sync is asserted for 10 ns per byte, it may not be possible to consistently detect the signal with a much slower clock of 33.3 MHz (30 ns), so data is to be hold temporarily and shifted later with a SLOAD signal which is asserted exactly one 30 ns SCLK period (SLOAD basically serves as a new data available signal).



Through the recovered signal of 100 MHz, data is shifted bit by bit into a serial to parallel shift register

We also need to detect the data for byte boundaries and once it is detected it generates a SYNCH signal at every 8 RCLK ticks. (for 10 ns per byte)

Ethernet synchronization.

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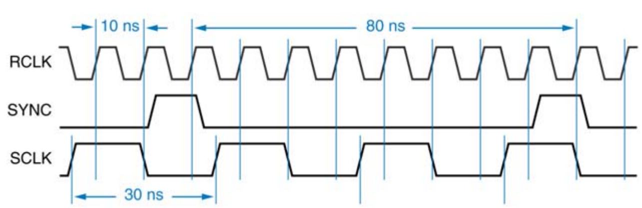
Ethernet Link & System Clock Timing



Ethernet link and system clock timing.

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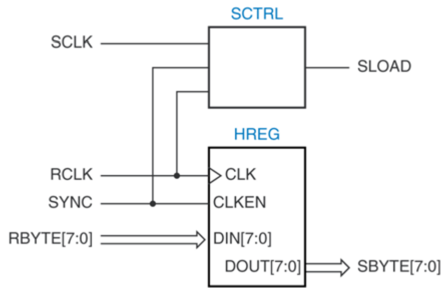
Byte Holding Register & Control



Byte holding register and control.

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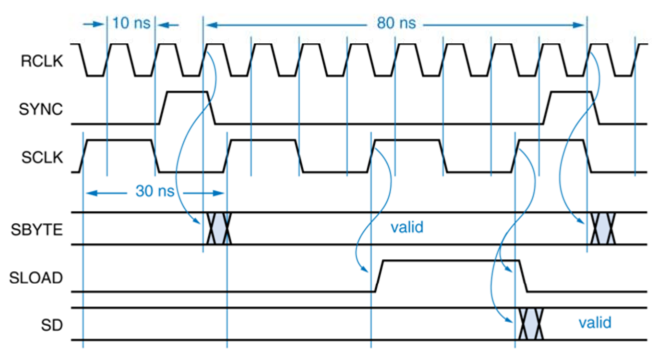
Timing



Timing for SBYTE and possible timing for SLOAD.

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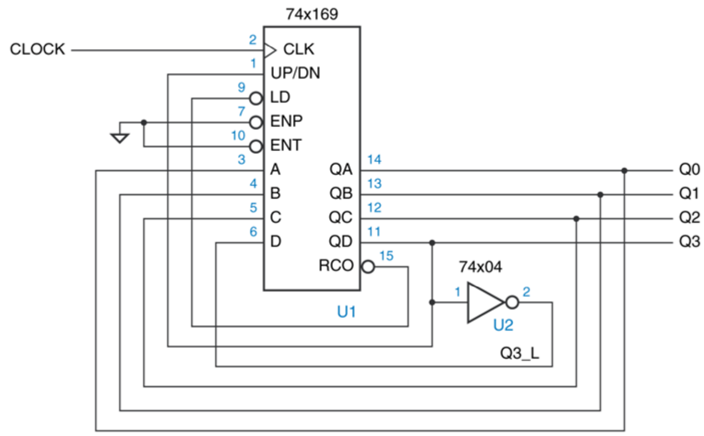
Counting Sequence



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