Diodes

Small Signal Model

Lecture # 2

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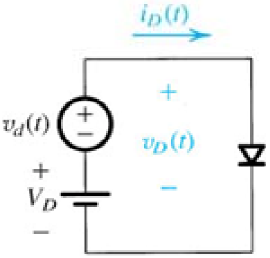
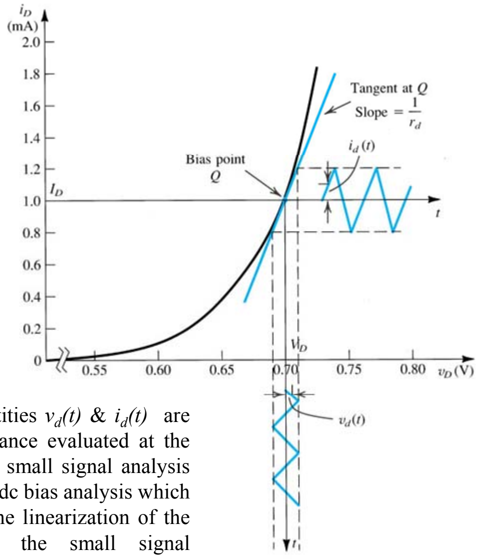
The Small Signal Model





The superimposed small signal quantities $v_d(t)$ & $i_d(t)$ are related by diodes small signal resistance evaluated at the bias point and the conclusion is that small signal analysis can be performed separately from the dc bias analysis which is a big convenience resulted from the linearization of the diode characteristics inherent in the small signal approximation.

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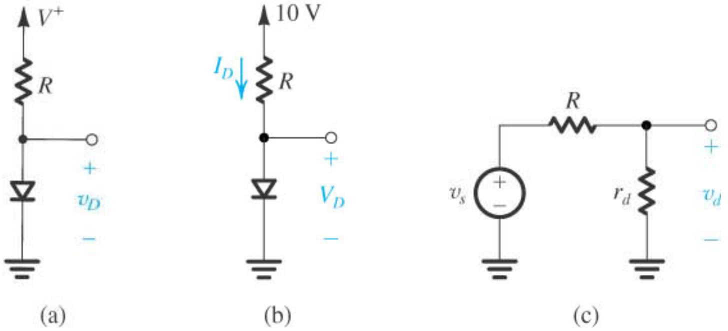
Example 3.6

Consider the following circuit (a), V = 10 V, R = 10K, a 60 Hz sinusoid of 1 V peak amplitude is superimposed, calculate the dc voltage of the diode and amplitude of the sine wave appearing across the diode, assuming the diode to have a 0.7 drop at 1 mA and n = 2.



$$I_D = \frac{V_{DD} - V_D}{R}$$

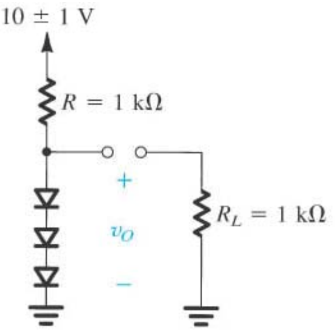
$$r_d = nV_T / I_D$$

$$v_d(peak) = v_S(peak)\frac{r_d}{R + r_d}$$

Figure 3.18 **(a)** Circuit for Example 3.6. **(b)** Circuit for calculating the dc operating point. **(c)** Small-signal equivalent circuit.

Example 3.7 (Voltage Regulation)

Consider the following circuit, 3 diodes provide 2.1 V constant (regulated), calculate the percentage change in the regulated voltage by varying (a) 10 % change in supply voltage (b) connecting a 1 K load resistor, assuming n = 2.



$$I_D = \frac{V_{DD} - V_D}{R}$$

$$r_d = nV_T / I_D$$

$$r = r_{d_1} + r_{d_2} + r_{d_3}$$

$$\Delta v_o = v_S(peak)\frac{r}{R + r}$$

Exercise 3.14

Find the value of the diode small signal resistance at a bias current of 0.1 mA, 1 mA and 10 mA, assume n = 1.

$$r_d = nV_T / I_D$$

Exercises 3.15

Consider a diode with n = 2 biased at 1 mA, find the change in current as a result of changing the voltage by;

(a) -20 mV
(b) -10 mV
(c) -5 mV
(d) +5 mV
(e) +10 mV
(f) +20 mV

For each case do the calculations using

(i) Small signal model
(ii) Exponential mode.

Small Signal Model

$$i_D = I_D + i_d$$

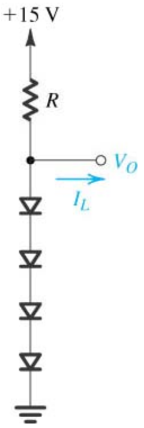
$$i_d = \frac{I_D}{nV_T} v_d$$

$$i_D = I_S e^{\frac{v_d}{nV_T}}$$

Exponential Model

Exercises 3.16

Design the following circuit so that $V_O = 3$ V, when $I_L = 0$ and V_O changes by 40 mV per 1 mA of load current. Find the value of R and the junction area of each diode (assume all four diodes are identical) relative to a diode of 0.7 V drop at 1 mA, assume n = 1.



$$\frac{\Delta v}{\Delta i} = \frac{40\,mV}{1\,mA} = ?$$

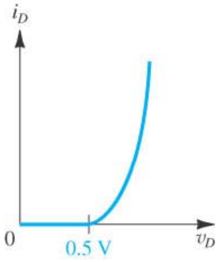
$$r_d = \frac{}{4}$$

$$I_D = nV_T / r_d$$

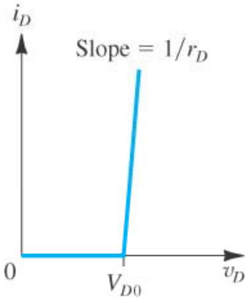
$$I_D = I_S e^{v_d / nV_T}$$

$$\frac{I_{D_2}}{I_{D1}} = \frac{I_{S_2}}{I_{S_1}} e^{\Delta v / nV_T}$$

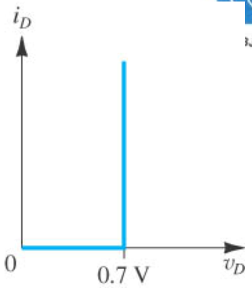
Summary of Diode Modelling



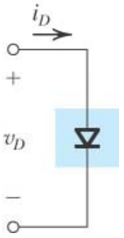
Exponential

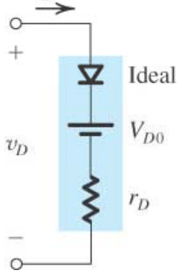


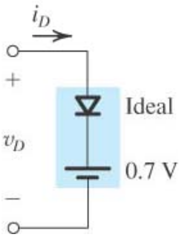
Piecewise Linear



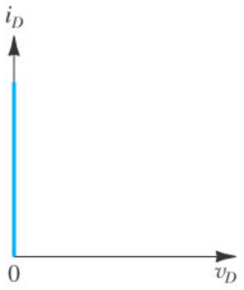
Constant Voltage Drop

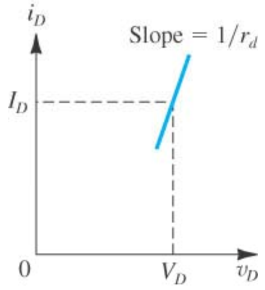






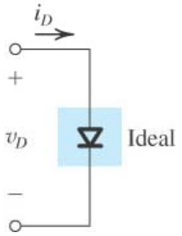
Summary

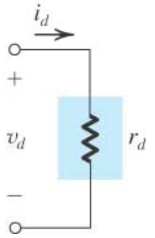




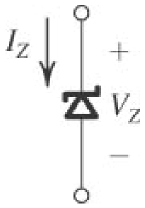
Ideal Diode Model

Small Signal Model

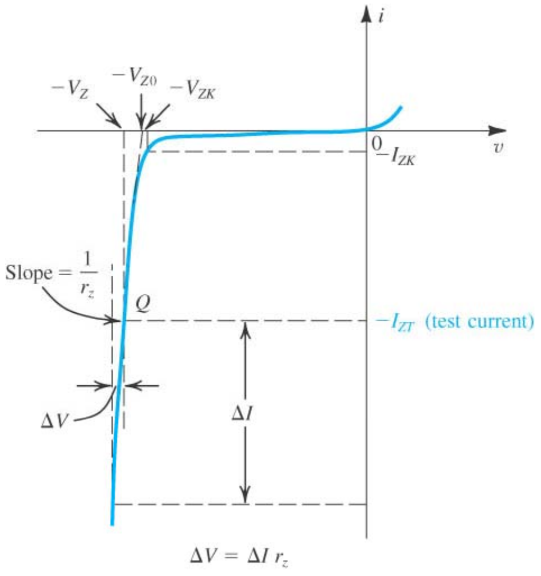




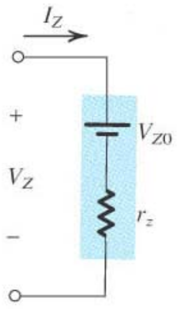
Voltage Regulation (Breakdown Region)

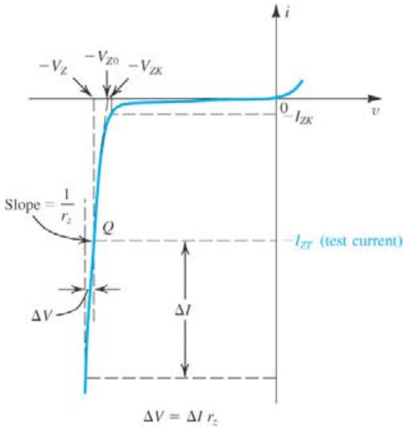


Zener Diode Characteristics



Zener Diode Modelling





$V_Z = V_{Z0} + r_Z\, I_Z$

$I_Z > I_{ZK}$ and $V_Z > V_{Z0}$

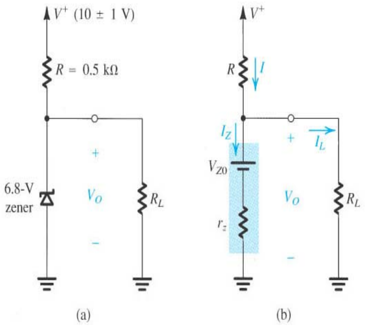
Example 3.8

$V_Z = 6.8$ V at $I_Z = 5$ mA, $r_Z = 20$ ohm and $I_{ZK} = 0.2$ mA, supply voltage is 10 V but can vary by ±1V.

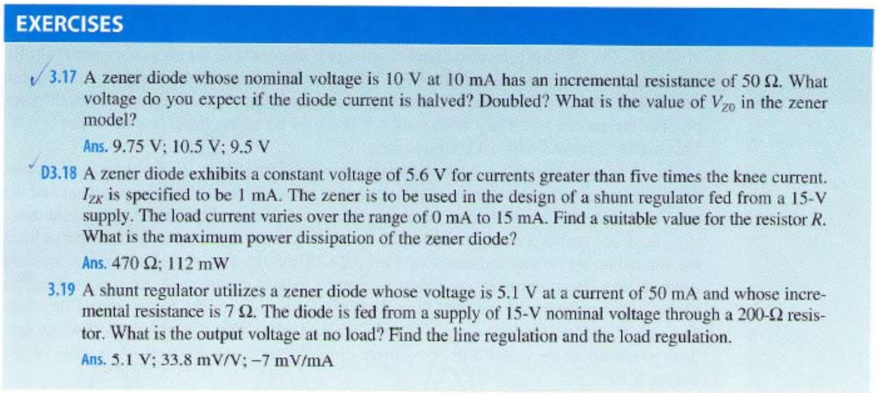
1. Find V_O with no load and supply voltage 10 V.
2. Find the change in V_O resulting from ±1V change. Note that $(\Delta V_O / \Delta V)$ usually expressed in mv/v as line regulation.
3. Find the change in V_O resulting from connecting load resistance R_L that draws I_L=1mA, hence find the load regulation $(\Delta V_O / \Delta I_L)$ in mV/mA.
4. Find the change in V_O when R_L =2 KΩ.
5. Find the change in V_O when R_L =5 KΩ.
6. What is the maximum value R_L for which the diode still operate in the breakdown region ?

$V_Z = V_{Z0} + r_Z\ I_Z$

$I_Z > I_{ZK}$ and $V_Z > V_{Z0}$



Exercises 3.17, 3.18 & 3.19



EXERCISES

✓ **3.17** A zener diode whose nominal voltage is 10 V at 10 mA has an incremental resistance of 50 Ω. What voltage do you expect if the diode current is halved? Doubled? What is the value of V_{Z0} in the zener model?

Ans. 9.75 V; 10.5 V; 9.5 V

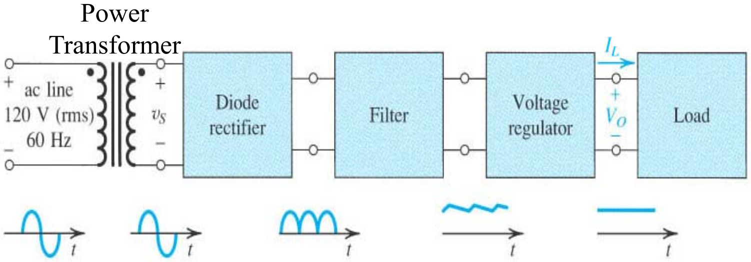
✓ **D3.18** A zener diode exhibits a constant voltage of 5.6 V for currents greater than five times the knee current. I_{ZK} is specified to be 1 mA. The zener is to be used in the design of a shunt regulator fed from a 15-V supply. The load current varies over the range of 0 mA to 15 mA. Find a suitable value for the resistor R. What is the maximum power dissipation of the zener diode?

Ans. 470 Ω; 112 mW

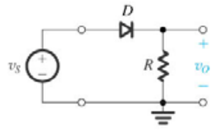
3.19 A shunt regulator utilizes a zener diode whose voltage is 5.1 V at a current of 50 mA and whose incremental resistance is 7 Ω. The diode is fed from a supply of 15-V nominal voltage through a 200-Ω resistor. What is the output voltage at no load? Find the line regulation and the load regulation.

Ans. 5.1 V; 33.8 mV/V; −7 mV/mA

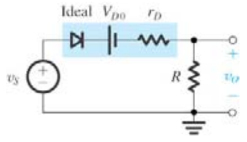
Rectifier Circuits



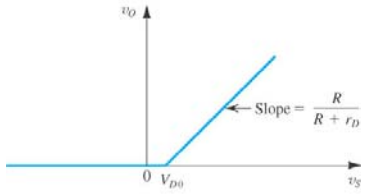
Half Wave Recitifier



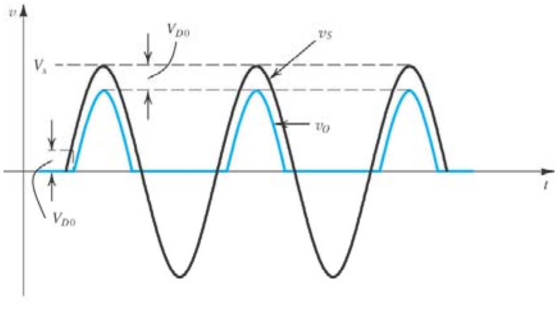
(a)



(b)



(c)



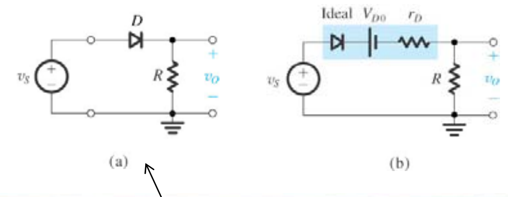
(d)

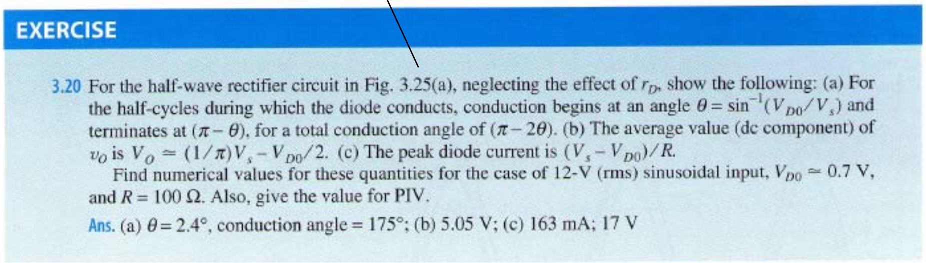
$v_0 = 0, \ v_S < V_{D0}$

$v_0 = (v_S - V_{D0})\ (R/R + r_D)\ ,\ v_S \geq V_{D0}$

$v_0 \approx v_S - V_{D0}$ because $r_D \ll R$

Exercise: 3.20





EXERCISE

3.20 For the half-wave rectifier circuit in Fig. 3.25(a), neglecting the effect of r_D, show the following: (a) For the half-cycles during which the diode conducts, conduction begins at an angle $\theta = \sin^{-1}(V_{D0}/V_s)$ and terminates at $(\pi - \theta)$, for a total conduction angle of $(\pi - 2\theta)$. (b) The average value (dc component) of v_O is $V_O \simeq (1/\pi)V_s - V_{D0}/2$. (c) The peak diode current is $(V_s - V_{D0})/R$.

Find numerical values for these quantities for the case of 12-V (rms) sinusoidal input, $V_{D0} \simeq 0.7$ V, and $R = 100\ \Omega$. Also, give the value for PIV.

Ans. (a) $\theta = 2.4°$, conduction angle = 175°; (b) 5.05 V; (c) 163 mA; 17 V

Full Wave Rectifier

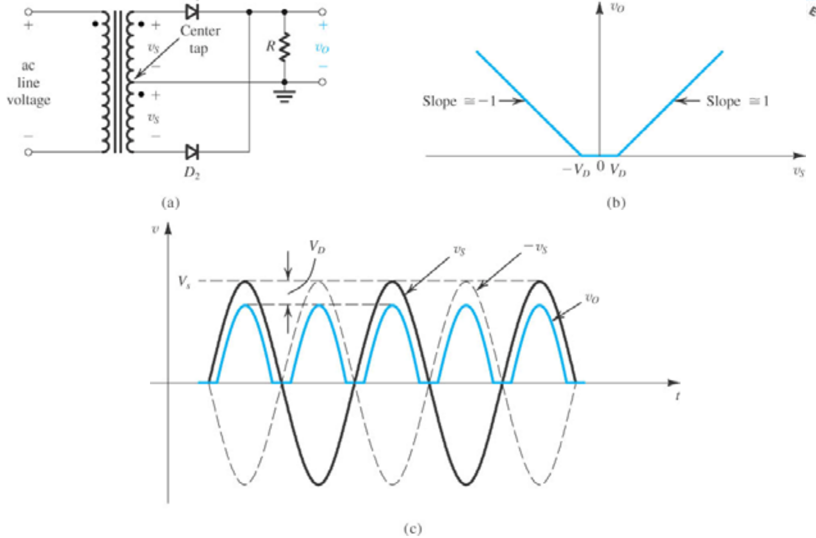
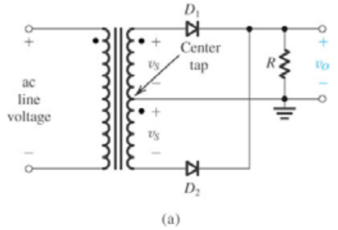


Figure 3.26 Full-wave rectifier utilizing a transformer with a center-tapped secondary winding: **(a)** circuit; **(b)** transfer characteristic assuming a constant-voltage-drop model for the diodes; **(c)** input and output waveforms.

Exercise 3.21

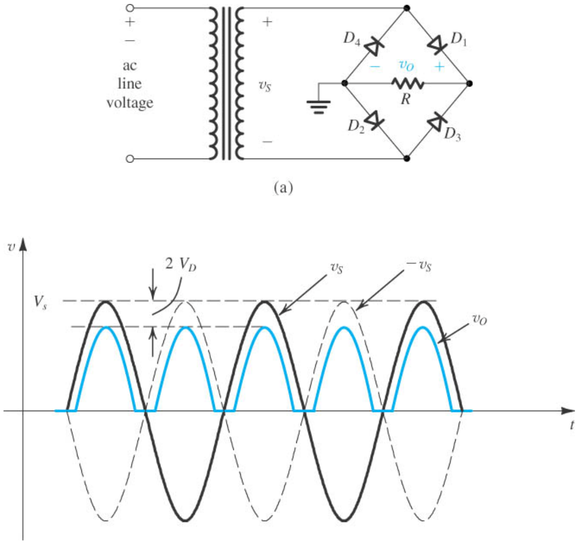


EXERCISE

3.21 For the full-wave rectifier circuit in Fig. 3.26(a), neglecting the effect of r_D, show the following: (a) The output is zero for an angle of $2\sin^{-1}(V_D/V_s)$ centered around the zero-crossing points of the sine-wave input. (b) The average value (dc component) of v_O is $V_O \simeq (2/\pi)V_s - V_D$. (c) The peak current through each diode is $(V_s - V_D)/R$. Find the fraction (percentage) of each cycle during which $v_O > 0$, the value of V_O, the peak diode current, and the value of PIV, all for the case in which v_S is a 12-V (rms) sinusoid, $V_D \simeq 0.7$ V, and $R = 100\ \Omega$.

Ans. 97.4%; 10.1 V; 163 mA; 33.2 V

Bridge Rectifier

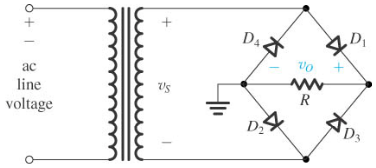


(a)

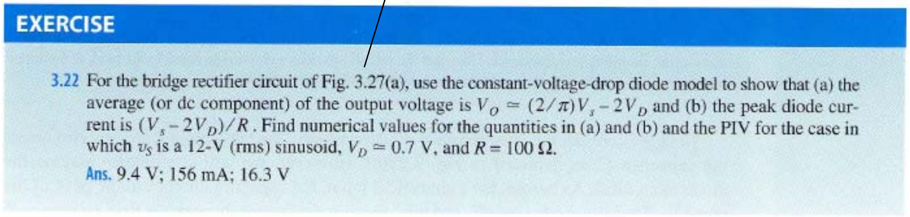
(b)

Figure 3.27 The bridge rectifier: **(a)** circuit, **(b)** input and output waveforms.

Exercise 3.22



(a)

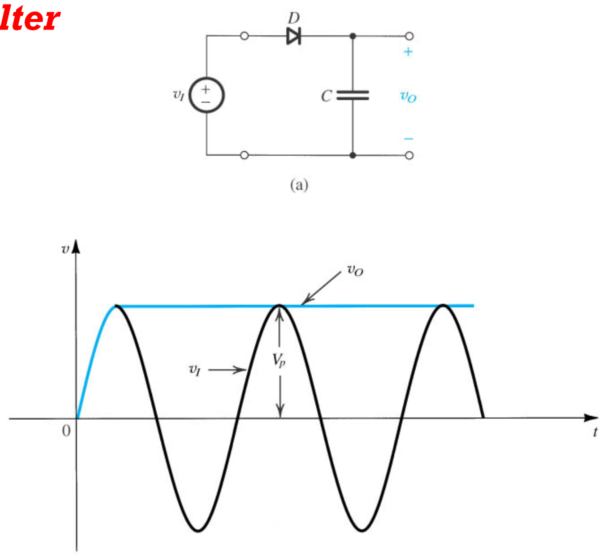


EXERCISE

3.22 For the bridge rectifier circuit of Fig. 3.27(a), use the constant-voltage-drop diode model to show that (a) the average (or dc component) of the output voltage is $V_O \simeq (2/\pi)V_s - 2V_D$ and (b) the peak diode current is $(V_s - 2V_D)/R$. Find numerical values for the quantities in (a) and (b) and the PIV for the case in which v_S is a 12-V (rms) sinusoid, $V_D \simeq 0.7$ V, and $R = 100\ \Omega$.

Ans. 9.4 V; 156 mA; 16.3 V

Capacitor Filter



(a)

(b)

Figure 3.28 **(a)** A simple circuit used to illustrate the effect of a filter capacitor. **(b)** Input and output waveforms assuming an ideal diode. Note that the circuit provides a dc voltage equal to the peak of the input sine wave. The circuit is therefore known as a peak rectifier or a peak detector.

Capacitor Filter (Realistic Situation)

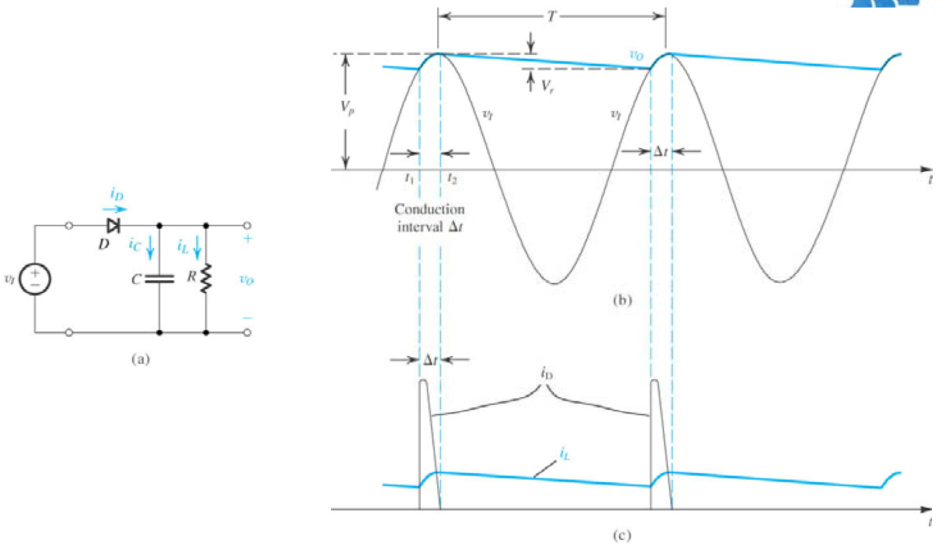


Figure 3.29 Voltage and current waveforms in the peak rectifier circuit with *CR* @ *T*. The diode is assumed ideal.

Full Wave Peak Rectifier

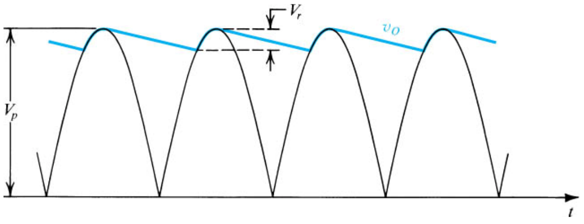
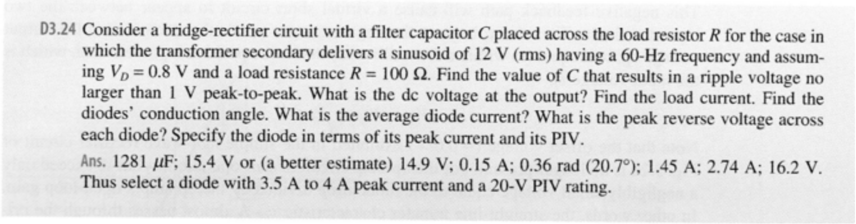


Figure 3.30 Waveforms in the full-wave peak rectifier.

Exercise 3.24



D3.24 Consider a bridge-rectifier circuit with a filter capacitor C placed across the load resistor R for the case in which the transformer secondary delivers a sinusoid of 12 V (rms) having a 60-Hz frequency and assuming $V_D = 0.8$ V and a load resistance $R = 100\ \Omega$. Find the value of C that results in a ripple voltage no larger than 1 V peak-to-peak. What is the dc voltage at the output? Find the load current. Find the diodes' conduction angle. What is the average diode current? What is the peak reverse voltage across each diode? Specify the diode in terms of its peak current and its PIV.

Ans. 1281 μF; 15.4 V or (a better estimate) 14.9 V; 0.15 A; 0.36 rad (20.7°); 1.45 A; 2.74 A; 16.2 V. Thus select a diode with 3.5 A to 4 A peak current and a 20-V PIV rating.

Super Diode (Precision Half Wave Rectifier)

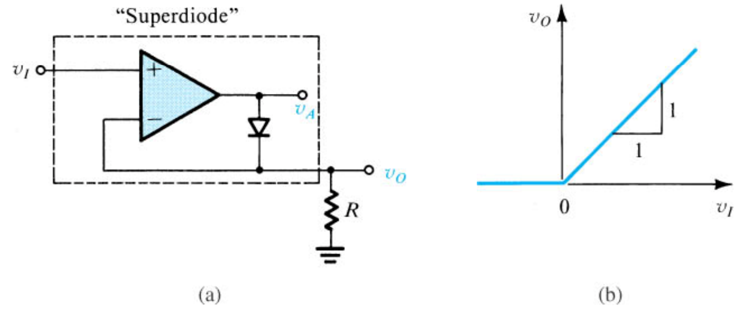
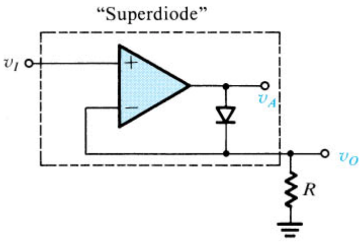
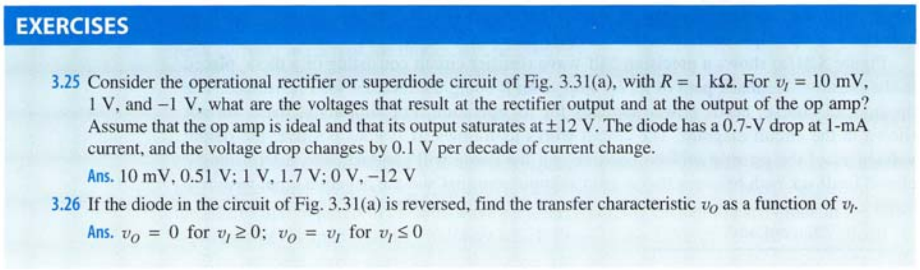


Figure 3.31 The "superdiode" precision half-wave rectifier and its almost-ideal transfer characteristic. Note that when $v_I > 0$ and the diode conducts, the op amp supplies the load current, and the source is conveniently buffered, an added advantage. Not shown are the op-amp power supplies.

Exercise 3.25 & 3.26



(a)



EXERCISES

3.25 Consider the operational rectifier or superdiode circuit of Fig. 3.31(a), with $R = 1\ \text{k}\Omega$. For $v_I = 10$ mV, 1 V, and −1 V, what are the voltages that result at the rectifier output and at the output of the op amp? Assume that the op amp is ideal and that its output saturates at ±12 V. The diode has a 0.7-V drop at 1-mA current, and the voltage drop changes by 0.1 V per decade of current change.

Ans. 10 mV, 0.51 V; 1 V, 1.7 V; 0 V, −12 V

3.26 If the diode in the circuit of Fig. 3.31(a) is reversed, find the transfer characteristic v_O as a function of v_I.

Ans. $v_O = 0$ for $v_I \geq 0$; $v_O = v_I$ for $v_I \leq 0$

Limiting & Clamping Circuits

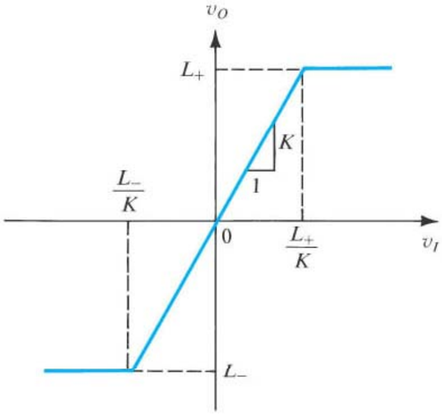


Figure 3.32 General transfer characteristic for a limiter circuit.

Clipper

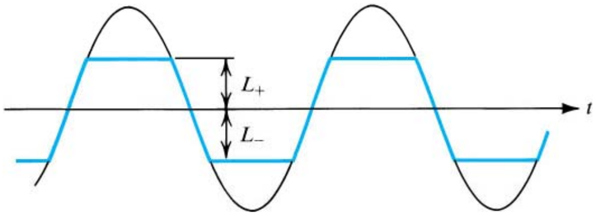
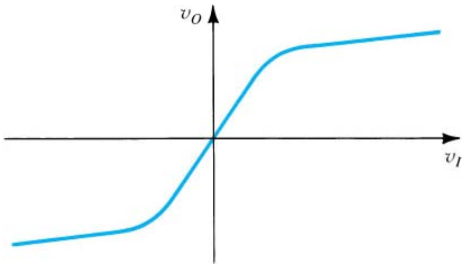


Figure 3.33 Applying a sine wave to a limiter can result in clipping off its two peaks.

Soft Limiter



Basic Limiting Circuits

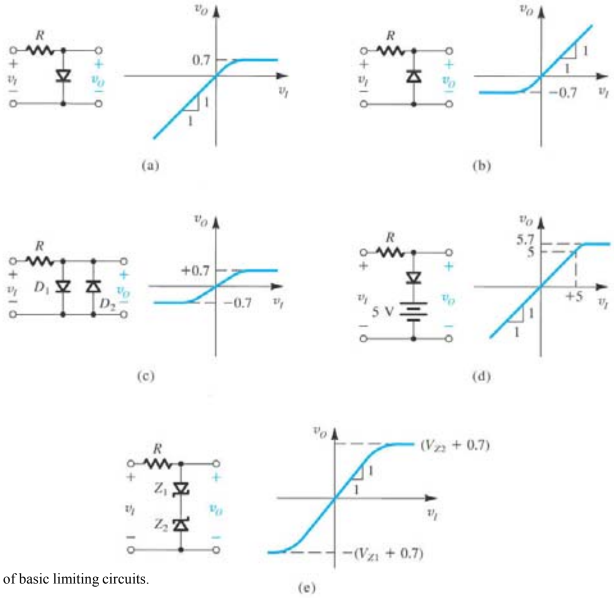
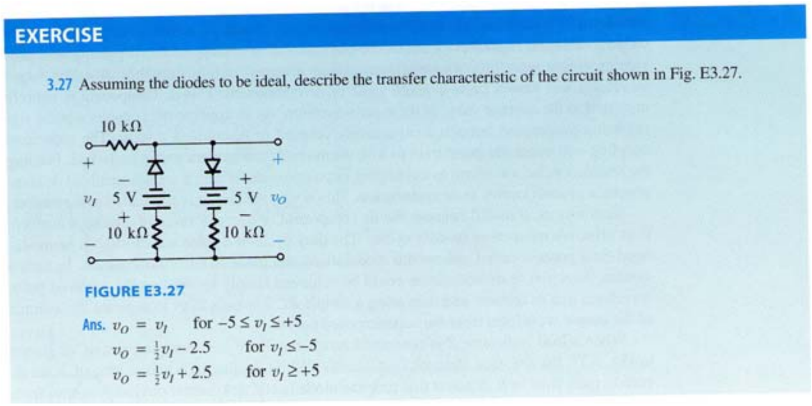


Figure 3.35 A variety of basic limiting circuits.

Exercise 3.27



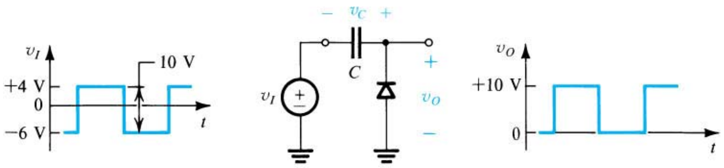
EXERCISE

3.27 Assuming the diodes to be ideal, describe the transfer characteristic of the circuit shown in Fig. E3.27.

FIGURE E3.27

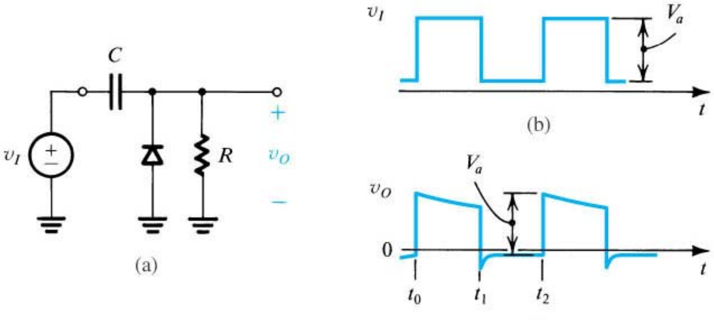
Ans. $v_O = v_I$ for $-5 \le v_I \le +5$
$v_O = \frac{1}{2}v_I - 2.5$ for $v_I \le -5$
$v_O = \frac{1}{2}v_I + 2.5$ for $v_I \ge +5$

Clamped Capacitor/ DC Restorer



(a) (b) (c)

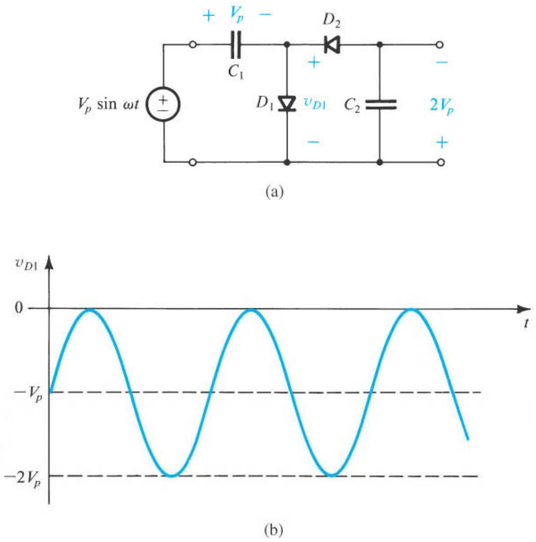
Clamped Capacitor with a Load Resistor



(a)

(c)

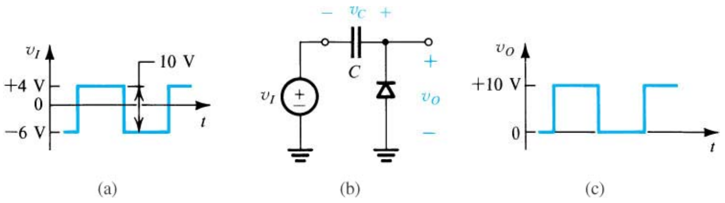
Volatge Doubler



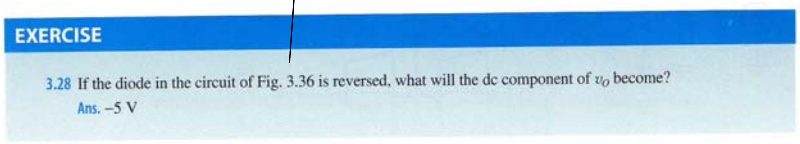
(a)

(b)

Exercise 3.28



(a) (b) (c)

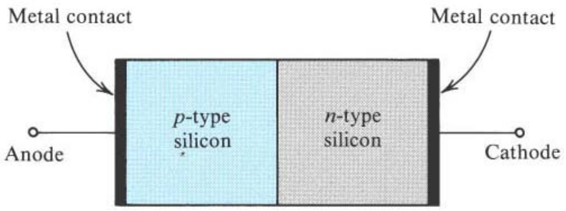


EXERCISE

3.28 If the diode in the circuit of Fig. 3.36 is reversed, what will the dc component of v_O become?

Ans. −5 V

Physical Structure of the Junction Diode



Silicon Crystal at Low Temperature

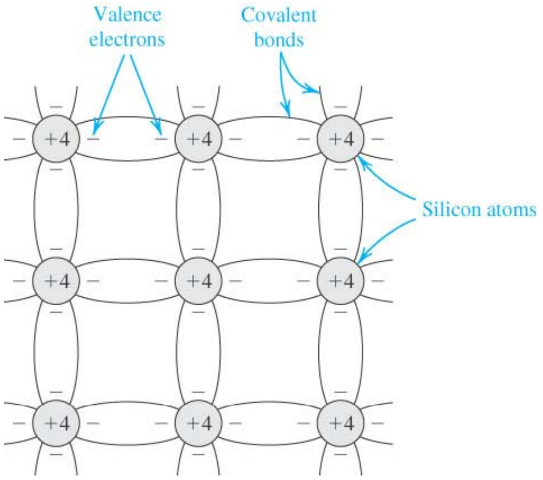


Figure 3.40 Two-dimensional representation of the silicon crystal. The circles represent the inner core of silicon atoms, with +4 indicating its positive charge of +4q, which is neutralized by the charge of the four valence electrons. Observe how the covalent bonds are formed by sharing of the valence electrons. At 0 K, all bonds are intact and no free electrons are available for current conduction.

Silicon Crystal at Room Temperature

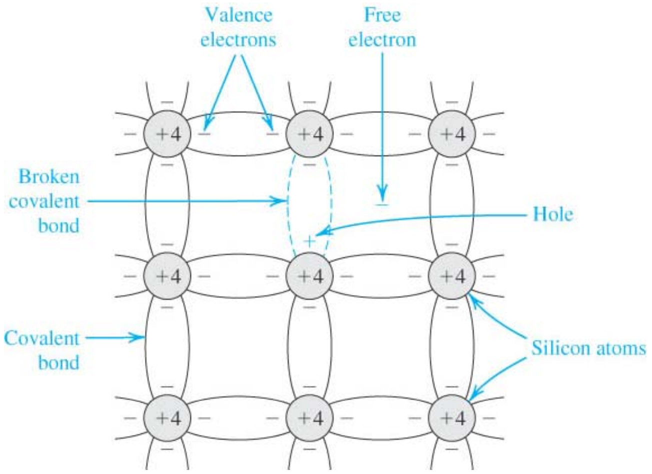
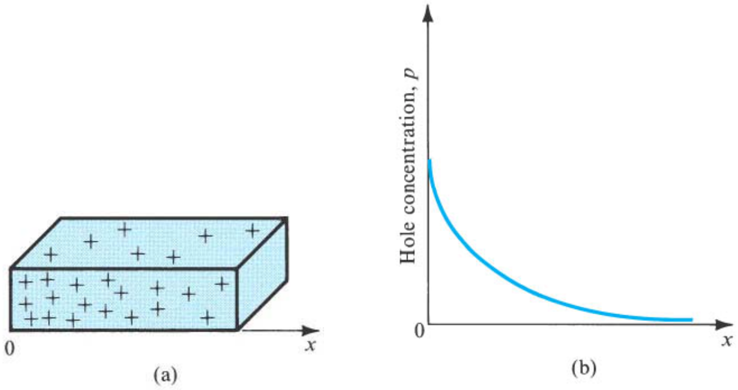


Figure 3.41 At room temperature, some of the covalent bonds are broken by thermal ionization. Each broken bond gives rise to a free electron and a hole, both of which become available for current conduction.

Drift & Diffusion



$$J_P = -qD_P \frac{dp}{dx}$$

$$J_{p-drift} = qp\mu_p E$$

$$v_{drift} = \mu_p E$$

$$J_{n-drift} = qp\mu_n E$$

Figure 3.42 A bar of intrinsic silicon **(a)** in which the hole concentration profile shown in **(b)** has been created along the *x*-axis by some unspecified mechanism.

Doped Semiconductor (n-type)

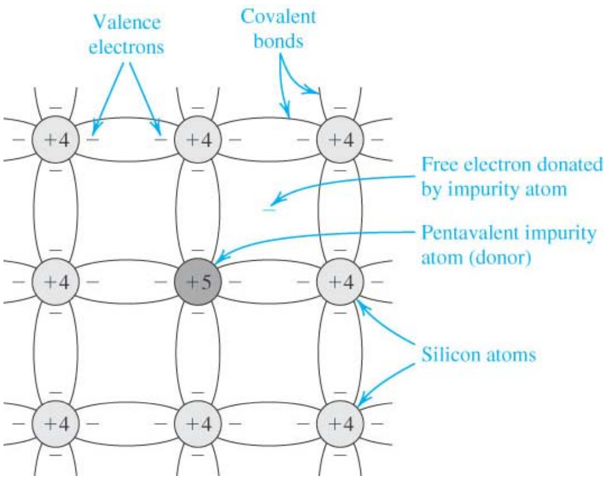


Figure 3.43 A silicon crystal doped by a pentavalent element. Each dopant atom donates a free electron and is thus called a donor. The doped semiconductor becomes *n* type.

Doped Semiconductor (p-type)

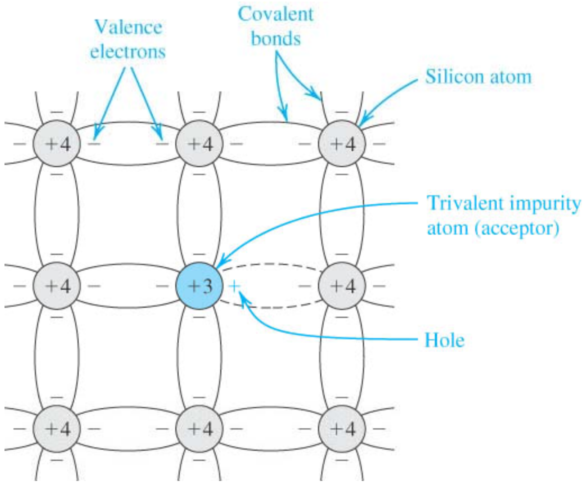
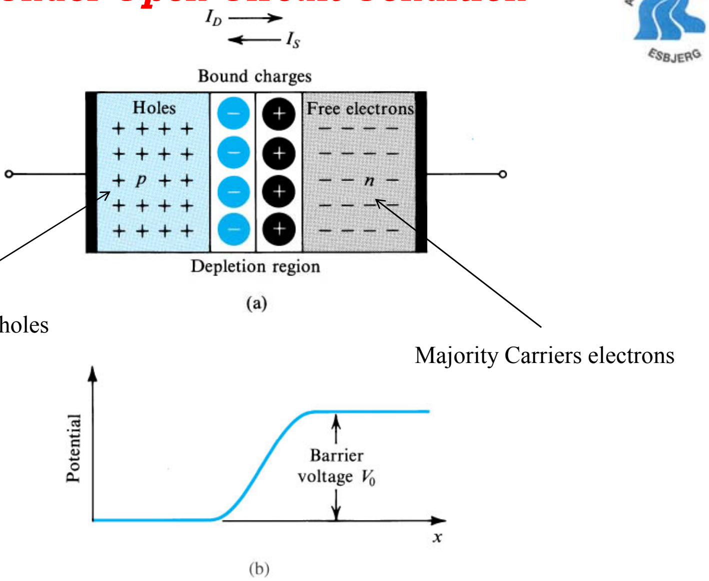


Figure 3.44 A silicon crystal doped with a trivalent impurity. Each dopant atom gives rise to a hole, and the semiconductor becomes *p* type.

pn Junction Under Open Circuit Condition



Majority Carriers holes

Majority Carriers electrons

Figure 3.45 **(a)** The *pn* junction with no applied voltage (open-circuited terminals). **(b)** The potential distribution along an axis perpendicular to the junction.

pn Junction Under Reverse Bias Condition

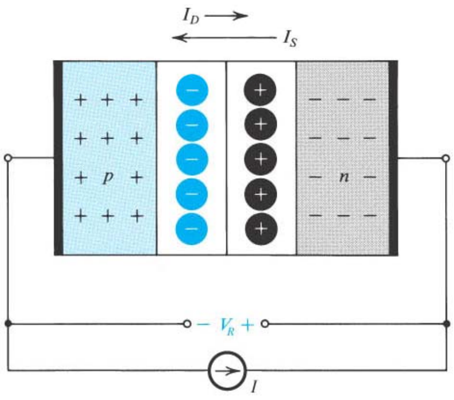


Figure 3.46 The *pn* junction excited by a constant-current source I in the reverse direction. To avoid breakdown, I is kept smaller than I_S. Note that the depletion layer widens and the barrier voltage increases by V_R volts, which appears between the terminals as a reverse voltage.

Depletion Capacitance

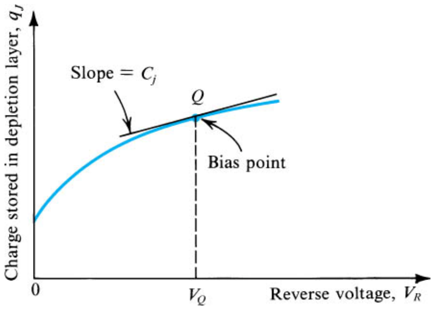


Figure 3.47 The charge stored on either side of the depletion layer as a function of the reverse voltage V_R.

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pn Junction in Breakdown Region

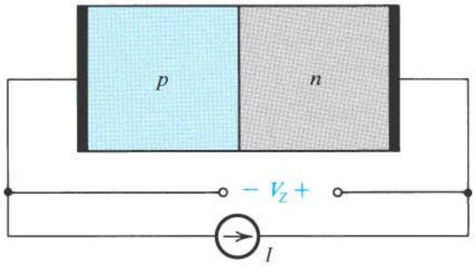

Figure 3.48 The *pn* junction excited by a reverse-current source *I*, where $I > I_S$. The junction breaks down, and a voltage V_Z, with the polarity indicated, develops across the junction.

Pn Junction Under Forward Bias Condition

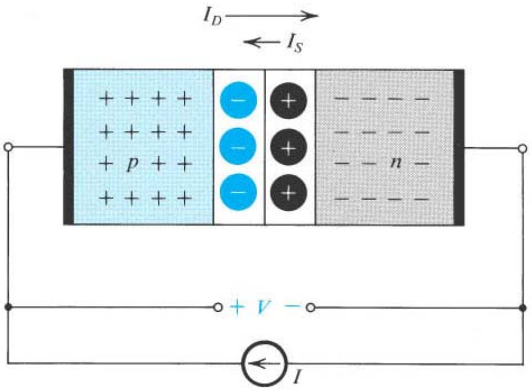

Figure 3.49 The *pn* junction excited by a constant-current source supplying a current *I* in the forward direction. The depletion layer narrows and the barrier voltage decreases by *V* volts, which appears as an external voltage in the forward direction.

Minority Carrier Distribution

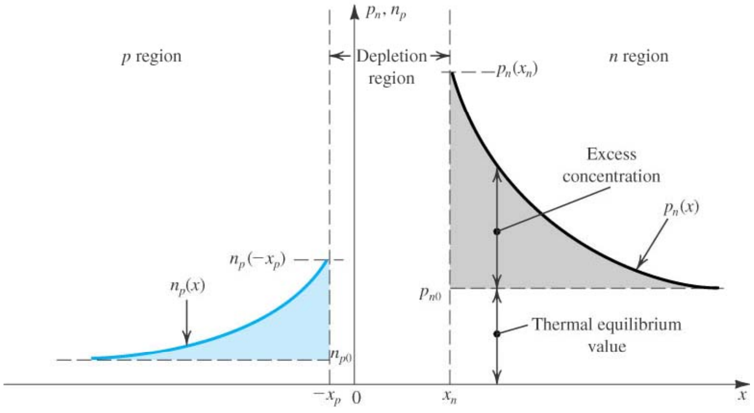

Figure 3.50 Minority-carrier distribution in a forward-biased *pn* junction. It is assumed that the *p* region is more heavily doped than the *n* region; N_A @ N_D.

Special Diodes

- Schottky Barrier Diode (SBD)
- Varactors
- Photo-Diodes
- Light Emitting Diodes

Home work:

Problems: 3.11, 3.12, 3.13, 3.14, 3.15, 3.16, 3.66, 3.67, 3.77, 3.78