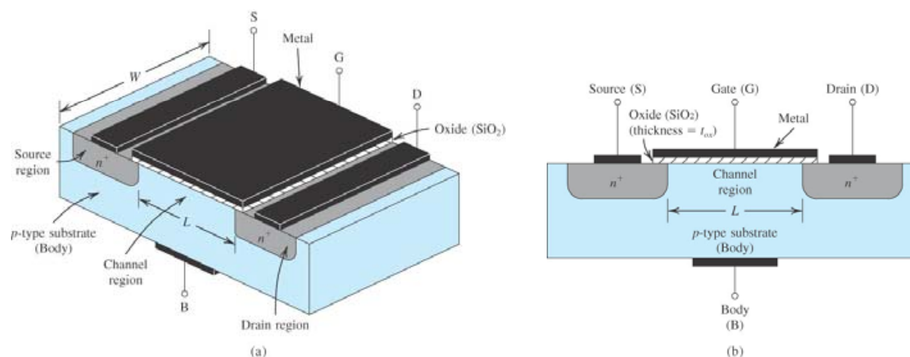
CHAPTER 4

MOS Field-Effect Transistors (MOSFETs)

Lecture # 3

MOSFET STRUCTURE



Voltage applied at the gate terminal controls the flow of current between source and drain and it flows longitudinally from drain to source in the areas called channel region.

Insulated Gate Device.

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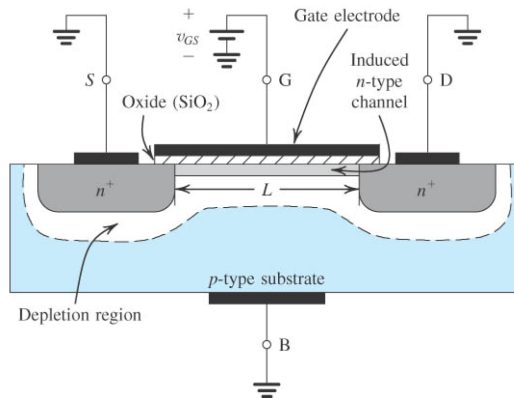
MOSFET OPERATION



When there is no bias voltage at Gate, resistance between Source & Drain is very high of the order of $10^{12}\ \Omega$.

The amount of voltage V_{GS} at which sufficient number of mobile electrons accumulates in the channel region, to form a conducting channel is called a threshold voltage.

An electric field is developed vertically. This is the field which controls the amount of charge in the channel and thus the amount of conduction in the channel. Reason of calling FET.

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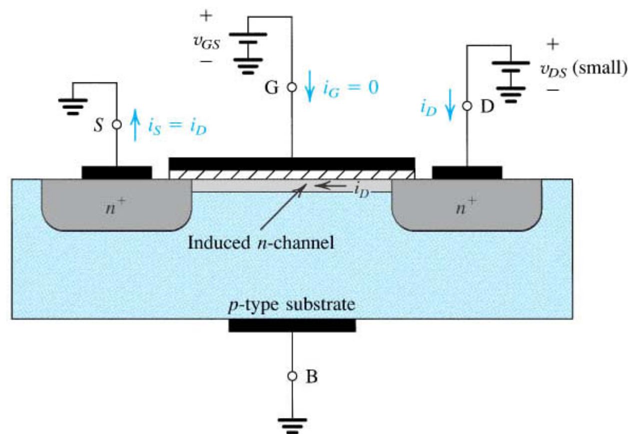
MOSFET OPERATION V_{DS}



Applying a small voltage V_{DS} between drain and source, so the current I_D flows from drain to source, the current will depend upon the density of electron in the channel which in reality depends on the amount of V_{GS}.

Current will be small (no current) until V_{GS} equal to V_T but as it will increase channel depth increases and so is the current.

Current I_D is proportional to $(V_{GS} – V_T)$ and of-course V_{DS} which causes I_D to flow.

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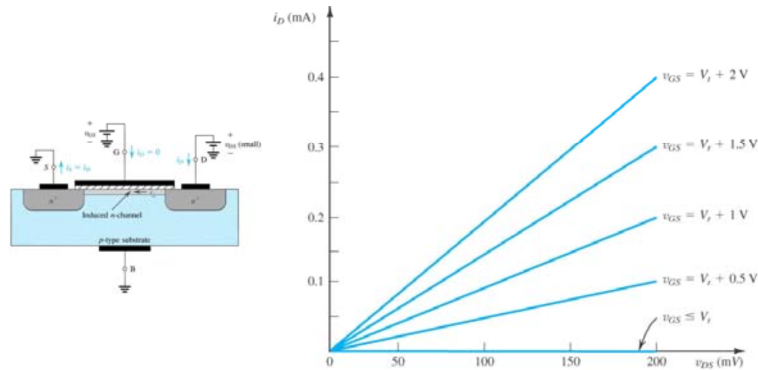
I_D - V_{DS} Characteristics



It can be seen that MOSFET acts as a linear resistor whose value is controlled by V_{GS}. The resistance is infinite when V_{GS} is equal or smaller than V_t.

Channel is enhanced with increasing V_{GS} . (Name Enhanced Mode Operation)

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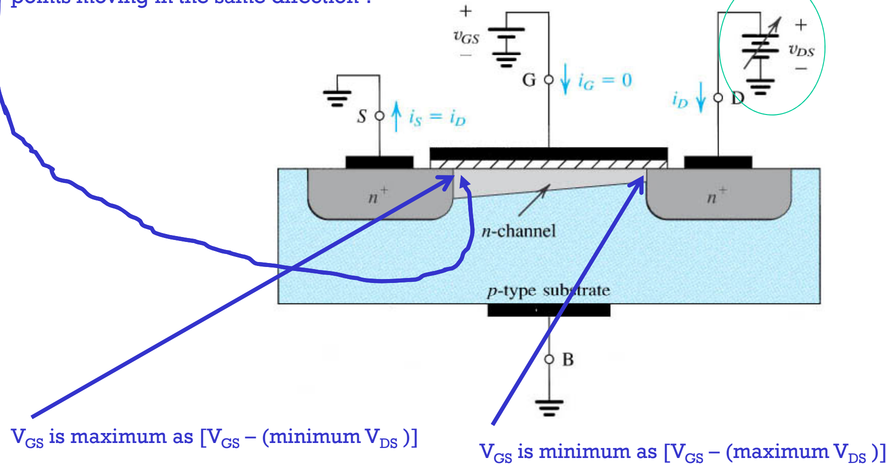
When V_{DS} is Increased

V_{DS} increases as you go along the channel from source to drain, measured with respect to source (from 0 to V_{DS}).

So what happens to gate potential along the channel at different points moving in the same direction ?



V_{GS} is maximum as [V_{GS} – (minimum V_{DS})]

V_{GS} is minimum as [V_{GS} – (maximum V_{DS})]

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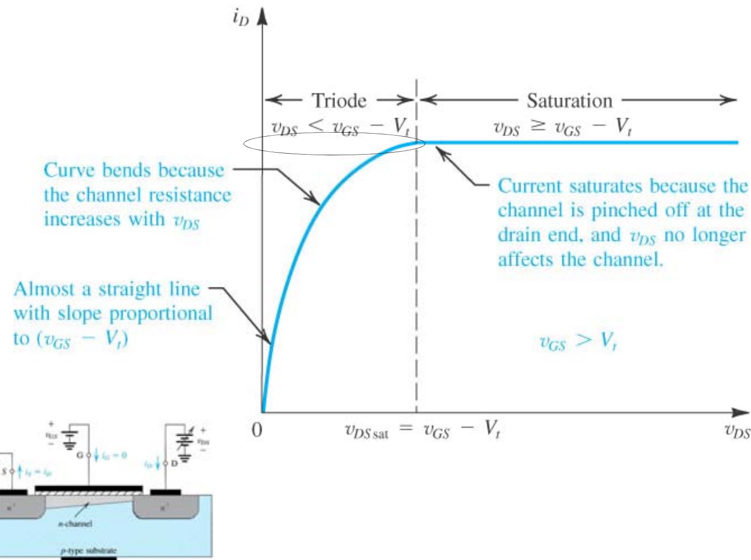
$I_D - V_{DS}$ Characteristics



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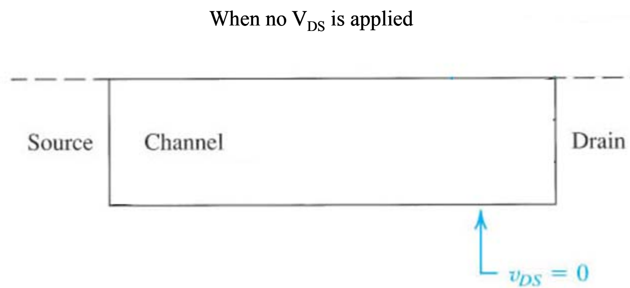
$V_{DSat} = V_{GS} - V_t$

When no V_{DS} is applied



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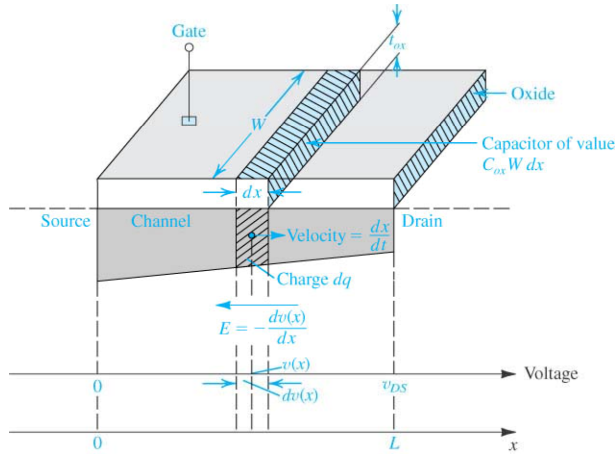
Derivation of $I_D - V_{DS}$ Characteristics



$C_{ox} = \varepsilon_{ox}/t_{ox}$ (ε_{ox} is the permittivity of the silicon oxide and t_{ox} is the thickness.).

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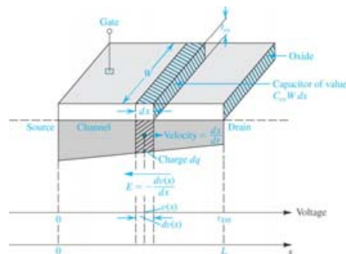
Derivation of $I_D - V_{DS}$ Characteristics



We have considred a very small strip at a distance x from the source. The capacitance of the strip is $C_{ox}Wdx$

To find the charge store in this strip we multiply it with effective voltage between the gate and the channel point x.

$$dq = -C_{ox}(Wdx)[v_{GS} - v(x) - v_t]$$

The voltage v_{DS} produce an electric field along the channel in the - ve direction.

$E(x) = -\frac{dv(x)}{dx}$ this field cause the charge to drift towards the drain with velocity *ds/dt*.

$$\frac{dx}{dt} = -\mu_n E(x) = \mu_n \frac{dv(x)}{dx} \qquad (\mu_n \text{ is the mobility of the electrons.})$$

Resulting drift current is $i = \frac{dq}{dt}$

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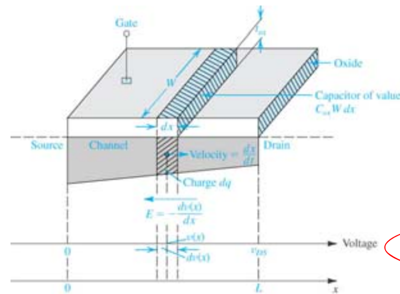
Derivation of $I_D - V_{DS}$ Characteristics



Rewriting $i = \frac{dq}{dx}\frac{dx}{dt}$ so we substitute all the values and we obtain :

$i = -\mu_n C_{ox} W [v_{GS} - v(x) - v_t] \frac{dv(x)}{dx}$ i is constant at all points and is equal to i_D

$i_D = -i = i_D = -i = \mu_n C_{ox} W [v_{GS} - v(x) - v_t] \frac{dv(x)}{dx}$

$i_D dx = \mu_n C_{ox} W [v_{GS} - v(x) - v_t] dv(x)$ Integrating both sides with x = 0 and x = L.

$$\int_0^L i_D dx = \int_0^{v_{DS}} \mu_n C_{ox} W [v_{GS} - v(x) - v_t] dv(x)$$

$$i_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[(v_{GS} - v_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$$ (Expression in Triode Region)

The expression for saturation region can be obtained by substituting $v_{DS} = v_{GS} - v_t$

$$i_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)\left[(v_{GS} - v_t)^2\right]$$ (Expression in Saturation Region)

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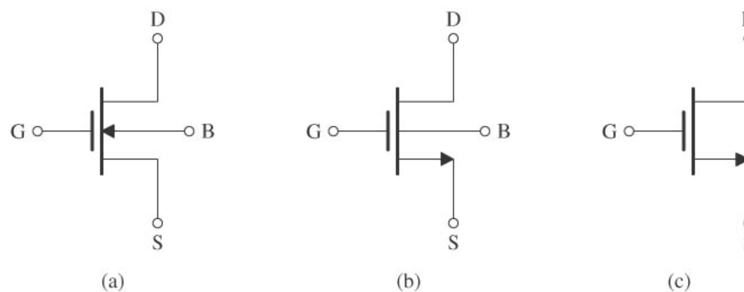
Circuit Symbol N Channel MOSFET



The voltage polarity determines the source and drain, basically, drain is always +ve relative to the source terminal in n type FET.

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P Channel MOSFET

The device operates in the same way as n-channel MOSFET, the difference is V_{GS} , V_t and V_{DS} are negative, also the current enters the source terminal and leaves drain terminal.

Note:
NMOS can be made smaller, so they operate faster.

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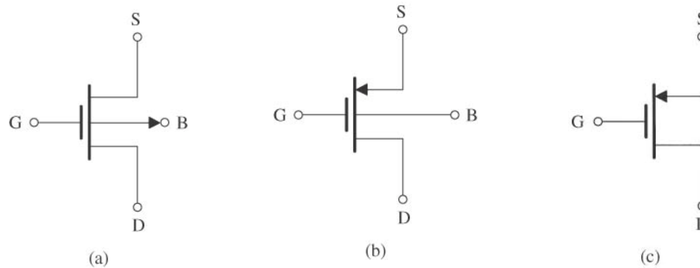
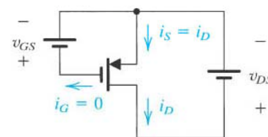
Circuit Symbol P Channel MOSFET





(d)

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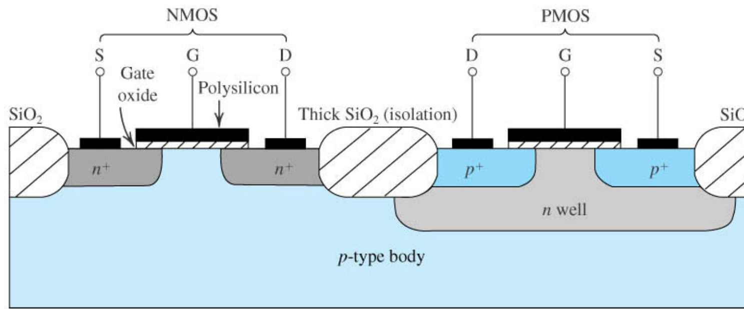
Complementary MOS (CMOS)



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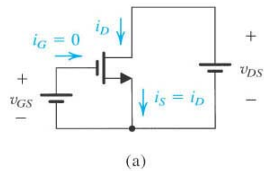
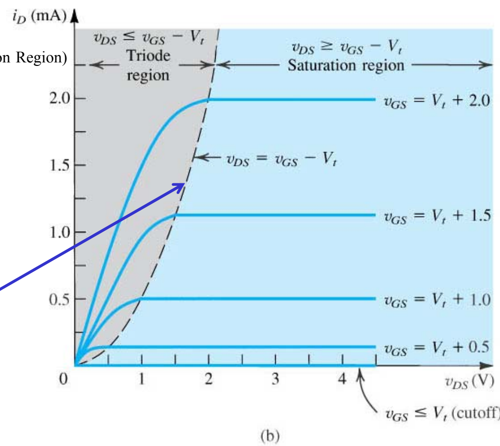
$I_D - V_{DS}$ Characteristics

$i_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[(v_{GS} - v_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$ (Expression in Triode Region)

$i_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)\left[(v_{GS} - v_t)^2\right]$ (Expression in Saturation Region)



(a)



(b)

$$i_D = \frac{1}{2} k_n' \frac{W}{L} v_{DS}^2$$

- FET as Switch (Cutoff and Triode Regions are used)
- FET as an Amplifier Saturation Region is used.

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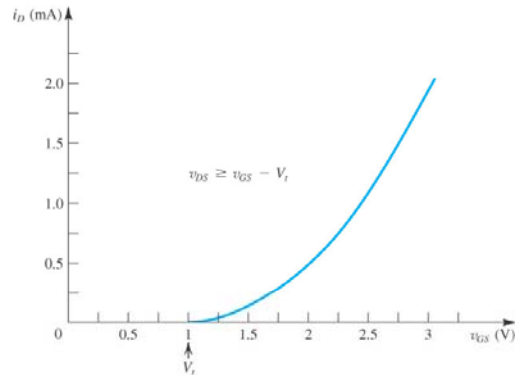
Drain Current (Square Law Equation) I_D

$$i_D = \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - v_t)^2$$



Drain current is independent of the drain voltage V_{DS}, basically it is determined by the gate voltage V_{GS} .

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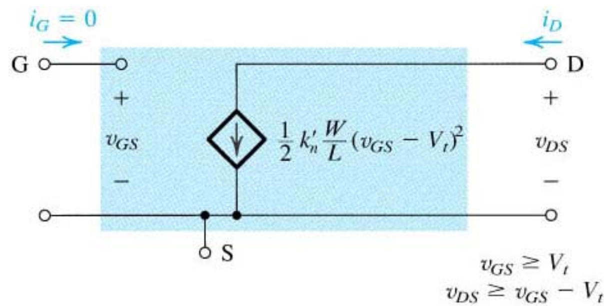
Equivalent Large Signal Circuit Model



As the drain current is independent of the drain voltage in the saturation region, and it behaves as an ideal current source whose value is controlled by V_{GS} .

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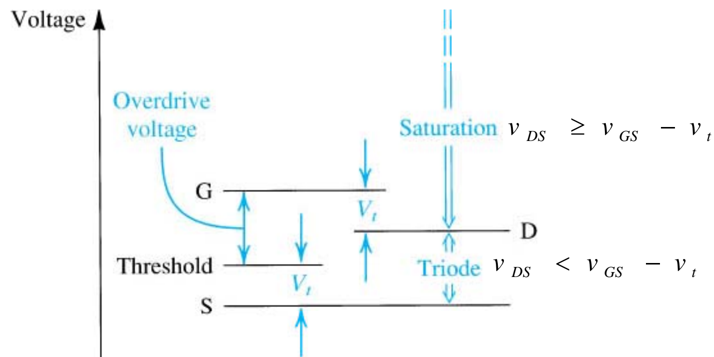
Relative Levels



$v_{DS} \geq v_{GS} - v_t$

$v_{DS} < v_{GS} - v_t$

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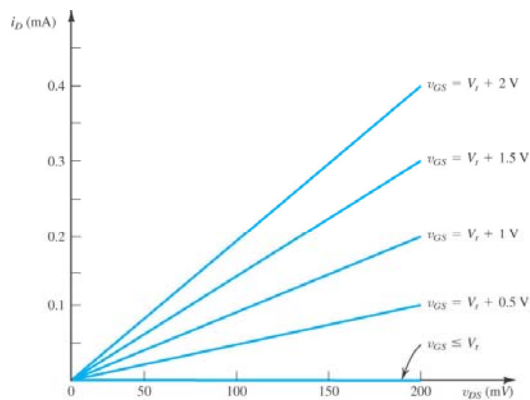
Exercise 4.1

4.1 From the description above of the operation of the MOSFET for small v_{DS}, we note that i_D is proportional to $(v_{GS} - V_t)v_{DS}$. Find the constant of proportionality for the particular device whose characteristics are depicted in Fig. 4.4. Also, give the range of drain-to-source resistances corresponding to an overdrive voltage, $v_{GS} - V_t$, of 0.5 V to 2 V.

Ans. 1 mA/V^2; 2 kΩ to 0.5 kΩ



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Exercises 4.2 & 4.3

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \qquad K_n' = \mu_n C_{ox}$$

4.2 For a 0.8-μm process technology for which $t_{ox} = 15$ nm and $\mu_n = 550$ cm^2/V·s, find C_{ox}, k_n', and the overdrive voltage $V_{OV} \equiv V_{GS} - V_t$ required to operate a transistor having $W/L = 20$ in saturation with $I_D = 0.2$ mA. What is the minimum value of V_{DS} needed?

Ans. 2.3 fF/μm^2; 127 μA/V^2; 0.40 V; 0.40 V

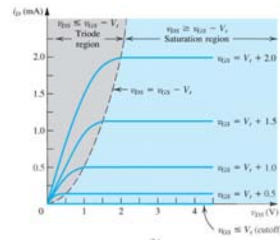
4.3 Use the expression for operation in the triode region to show that an n-channel MOSFET operated with an overdrive voltage $V_{OV} \equiv V_{GS} - V_t$ and having a small V_{DS} across it behaves approximately as a linear resistance r_{DS},

$$r_{DS} = 1\Big/\left[k_n' \frac{W}{L} V_{OV}\right]$$

Calculate the value of r_{DS} obtained for a device having $k_n' = 100$ μA/V^2 and $W/L = 10$ when operated with an overdrive voltage of 0.5 V.

Ans. 2 kΩ

$$i_D = k_n' \frac{W}{L}\left[(v_{GS} - v_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$$



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Exercises 4.4, 4.5 & 4.6

4.4 An enhancement-type NMOS transistor with $V_t = 0.7$ V has its source terminal grounded and a 1.5-V dc applied to the gate. In what region does the device operate for (a) $V_D = +0.5$ V? (b) $V_D = 0.9$ V? (c) $V_D = 3$ V?

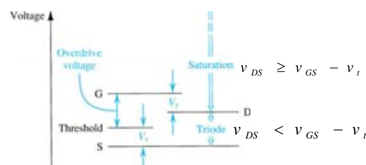
Ans. (a) Triode; (b) Saturation; (c) Saturation

4.5 If the NMOS device in Exercise 4.4 has $\mu_n C_{ox} = 100$ μA/V^2, $W = 10$ μm, and $L = 1$ μm, find the value of drain current that results in each of the three cases (a), (b), and (c) specified in Exercise 4.4.

Ans. (a) 275 μA; (b) 320 μA; (c) 320 μA

4.6 An enhancement-type NMOS transistor with $V_t = 0.7$ V conducts a current $i_D = 100$ μA when $v_{GS} = v_{DS} = 1.2$ V. Find the value of i_D for $v_{GS} = 1.5$ V and $v_{DS} = 3$ V. Also, calculate the value of the drain-to-source resistance r_{DS} for small v_{DS} and $v_{GS} = 3.2$ V.

Ans. 256 μA; 500 Ω



$v_{DS} \geq v_{GS} - v_t$

$v_{DS} < v_{GS} - v_t$

$$i_D = k_n' \frac{W}{L}\left[(v_{GS} - v_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

$$i_D = \frac{1}{2} k_n' \frac{W}{L}(v_{GS} - v_t)^2$$

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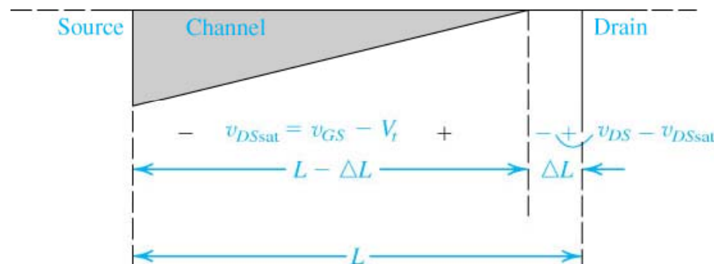
Finite Output Resistance in Saturation



Increasing V_{DS} beyond V_{DSat} has some affect on the drain current, if we look at the equation:

$$i_D = \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - v_t)^2$$

we can see that the drain current is inversely proportional to the channel length and as channel length decreases current will increase.

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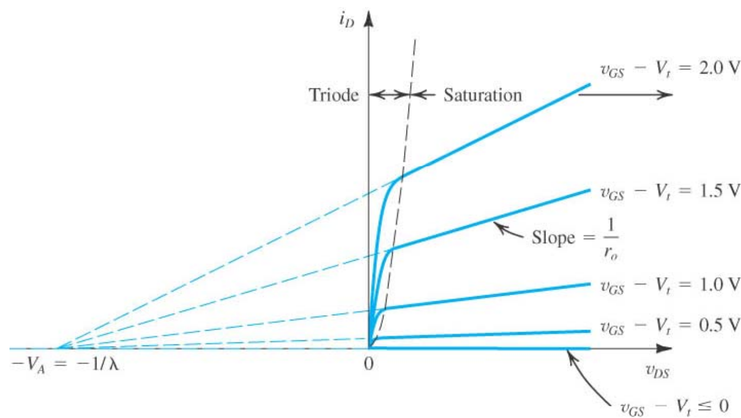
Effect of V_{DS} on I_D in the Saturation Region



$$i_D = \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - v_t)^2 (1 + \lambda v_{DS})$$

λ is a process technology parameter with dimensions of V^{-1} and that for a given process λ is inversely proportional to the length selected for the channel.

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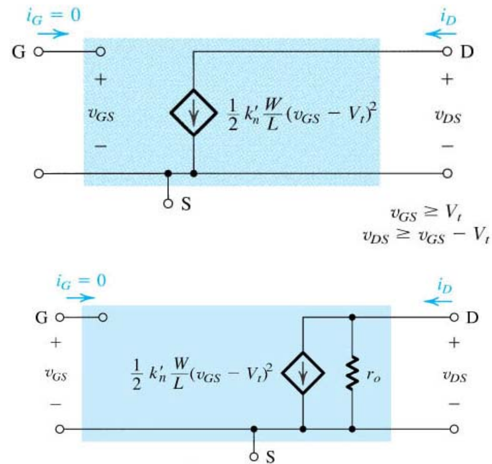
Equivalent Circuit Model with Resistance



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Exercise 4.7

4.7 An NMOS transistor is fabricated in a 0.4-μm process having $\mu_n C_{ox} = 200\ \mu A/V^2$ and $V_A' = 50\ V/\mu m$ of channel length. If $L = 0.8\ \mu m$ and $W = 16\ \mu m$, find V_A and λ. Find the value of I_D that results when the device is operated with an overdrive voltage $V_{OV} = 0.5$ V and $V_{DS} = 1$ V. Also, find the value of r_o at this operating point. If V_{DS} is increased by 2 V, what is the corresponding change in I_D?

Ans. 40 V; 0.025 V^{-1}; 0.51 mA; 80 kΩ; 0.025 mA

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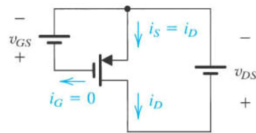
P-Channel MOSFET

$v_{GS} \le v_t$ (To induce a channel)

Equivalently $v_{SG} \ge |v_t|$



(d)

$v_{DS} = (v_{GS} - v_t)$ (Continous channel)

$$i_D = k_p' \frac{W}{L}[(v_{GS} - v_t)v_{DS} - \frac{1}{2}v_{DS}^2]$$

$$i_D = \frac{1}{2}k_p' \frac{W}{L}(v_{GS} - v_t)^2(1 + \lambda v_{DS})$$

(Pinched off channel)

$v_{GS}, v_t, \lambda, v_{DS}$ are all - ve.

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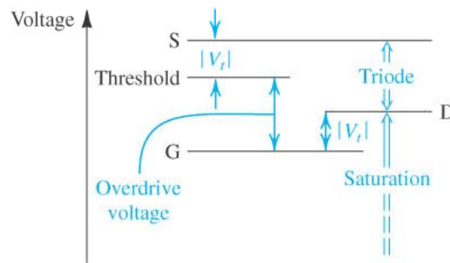
Voltage Levels



Every thing is reversed compared with NMOS

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Exercise 4.8

√ 4.8 The PMOS transistor shown in Fig. E4.8 has $V_t = -1$ V, $k'_p = 60\ \mu A/V^2$, and $W/L = 10$. (a) Find the range of V_G for which the transistor conducts. (b) In terms of V_G, find the range of V_D for which the transistor operates in the triode region. (c) In terms of V_G, find the range of V_D for which the transistor operates in saturation. (d) Neglecting channel-length modulation (i.e., assuming $\lambda = 0$), find the values of $|V_{OV}|$ and V_G and the corresponding range of V_D to operate the transistor in the saturation mode with $I_D = 75\ \mu A$. (e) If $\lambda = -0.02\ V^{-1}$, find the value of r_o corresponding to the overdrive voltage determined in (d). (f) For $\lambda = -0.02\ V^{-1}$ and for the value of V_{OV} determined in (d), find I_D at $V_D = +3$ V and at $V_D = 0$ V; hence, calculate the value of the apparent output resistance in saturation. Compare to the value found in (e).

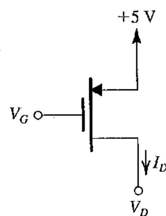

FIGURE E4.8

From PMOS we know that $V_{SG} \geq |V_t|$

In Triode $V_{DS} \geq (V_{GS} - V_t)$

In Saturation $V_{DS} \leq (V_{GS} - V_t)$

Ans. (a) $V_G \leq +4$ V; (b) $V_D \geq V_G + 1$; (c) $V_D \leq V_G + 1$; (d) 0.5 V, 3.5 V, ≤4.5 V; (e) 0.67 MΩ; (f) 78 μA, 82.5 μA, 0.67 MΩ (same).

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Exercise 4.9

√4.9 An NMOS transistor has $V_{t0} = 0.8$ V, $2\phi_f = 0.7$ V, and $\gamma = 0.4\ V^{1/2}$. Find V_t when $V_{SB} = 3$ V.
Ans. 1.23 V

$$v_t = v_{t0} + \gamma[\sqrt{2\varphi_f + v_{SB}} - \sqrt{2\varphi_f}\,]$$

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Temperature Effect

$$i_D = \frac{1}{2} k'_n \frac{W}{L} (v_{GS} - v_t)^2$$

Both K'_n and V_t are temperature sensitive:

- Typically V_t decreases by 2 mV per degree rise in temperature, so it will increase the current.
- However, K'_n decreases with increase in temperature and it is dominating one so the over all effect is that drain current decreases with increase in temperature.

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Breakdown & Input Protection

When the drain voltage reaches at a point when the breakdown occurs (avalanche) at about 20 V to 150 V. In some devices breakdown can occur at lower voltage 20 if the channel length is small. So the drain current increases rapidly.

Another type of breakdown can also occur if the gate to source voltage exceeds 30 V, this basically is the breakdown of the gate oxide which means permanent damage to the IC. It may seem 30 V very high but as the input resistance of the MOSFET is very high and the input capacitance is very small so a small amount of static charge at the input can cause the breakdown voltage to be exceeded.

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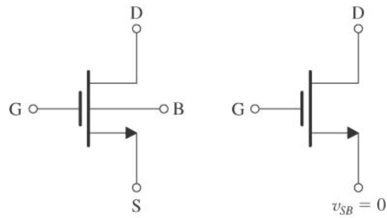
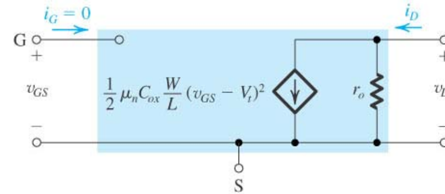
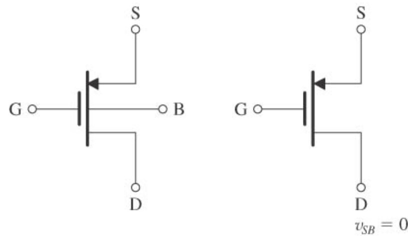
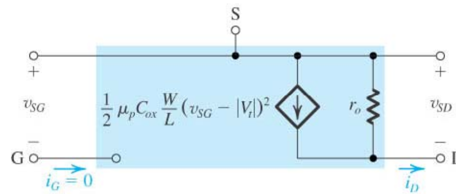
Summary









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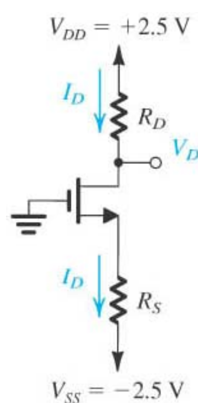
Example 4.2

Design the circuit of Fig. 4.20 so that the transistor operates at $I_D = 0.4$ mA and $V_D = +0.5$ V. The NMOS transistor has $V_t = 0.7$ V, $\mu_n C_{ox} = 100\ \mu\text{A/V}^2$, $L = 1\ \mu$m, and $W = 32\ \mu$m. Neglect the channel-length modulation effect (i.e., assume that $\lambda = 0$).

As $V_D = 0.5$ is greater than $V_G = 0$, so it is working in saturation.



$$I_D = \frac{1}{2}\mu_n c_{ox}\frac{W}{L}(v_{GS} - v_t)^2$$

$$400 = \frac{1}{2} \times 100 \times \frac{32}{1} \times v_{ov}^2$$

$$v_{ov} = 0.5 v$$

$$v_{GS} = v_t + v_{ov} = 0.7 + 0.5 = 1.2 v$$

As gate is at 0 potential so source must be at -1.2 v

$$R_S = \frac{v_S - v_{SS}}{I_D} = \frac{-1.2 - (-2.5)}{0.4} = 3.25\ K\Omega$$

$$R_D = \frac{v_{DD} - v_D}{I_D} = \frac{2.5 - 0.5}{0.4} = 5.0\ K\Omega$$

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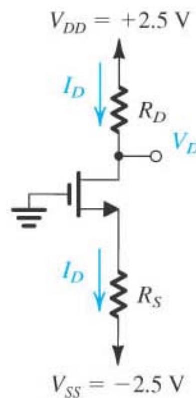
Exercise 4.10

✓ **D4.10** Redesign the circuit of Fig. 4.20 for the following case: $V_{DD} = -V_{SS} = 2.5$ V, $V_t = 1$ V, $\mu_n C_{ox} = 60\ \mu A/V^2$, $W/L = 120\ \mu m/3\ \mu m$, $I_D = 0.3$ mA, and $V_D = +0.4$ V.

Ans. $R_S = 3.3$ kΩ; $R_D = 7$ kΩ



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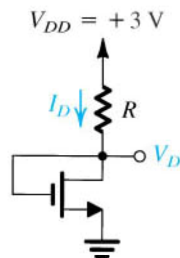
Example 4.3

Design the circuit in Fig. 4.21 to obtain a current I_D of 80 μA. Find the value required for R, and find the dc voltage V_D. Let the NMOS transistor have $V_t = 0.6$ V, $\mu_n C_{ox} = 200\ \mu A/V^2$, $L = 0.8\ \mu m$, and $W = 4\ \mu m$. Neglect the channel-length modulation effect (i.e., assume $\lambda = 0$).



Same way as you calculated the value of over drive voltage using the square law equation in the previous example.

$$I_D = \frac{1}{2}\mu_n c_{ox}\frac{W}{L}(v_{GS} - v_t)^2$$

You can see that the drain and gate are conected so after calculating the over drive voltage you can use the relationship to calculate V_{GS} and then V_G and V_D.

$$v_{GS} = v_t + v_{ov} = 0.6 + 0.4 = 1.0v$$
$$v_D = v_G = +1.0v$$

Now you can calculate R as:

$$R = \frac{v_{DD} - v_D}{I_D} = \frac{3.0 - 1.0}{0.080} = 25\ K\Omega$$

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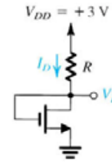
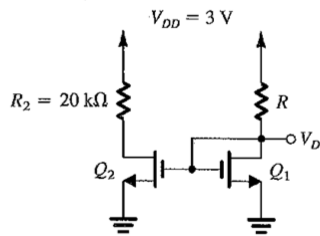
Exercise 4.11 & 4.12

D4.11 Redesign the circuit in Example 4.3 to double the value of I_D without changing V_D. Give new values for W/L and R.

Ans. $W/L = 10$, say 8 μm/0.8 μm; $R = 12.5$ kΩ



4.12 Consider the circuit of Fig. 4.21, which is designed in Example 4.3 (to which you should refer before solving this problem). Let the voltage V_D be applied to the gate of another transistor Q_2, as shown in Fig. E4.12. Assume that Q_2 is identical to Q_1. Find the drain current and voltage of Q_2. (Assume $\lambda = 0$.)



V_D = 1 from example 4.3

Ans. 80 μA; +1.4 V

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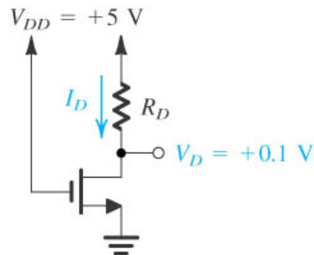
Example 4.4

Design the circuit in Fig. 4.22 to establish a drain voltage of 0.1 V. What is the effective resistance between drain and source at this operating point? Let $V_t = 1$ V and $k_n'(W/L) = 1$ mA/V^2.



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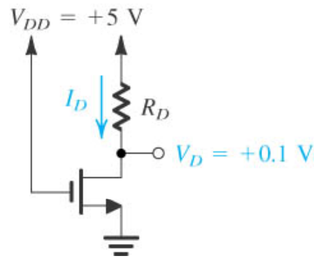
Exercise 4.13

4.13 If in the circuit of Example 4.4 the value of R_D is doubled, find approximate values for I_D and V_D.

Ans. 0.2 mA; 0.05 V



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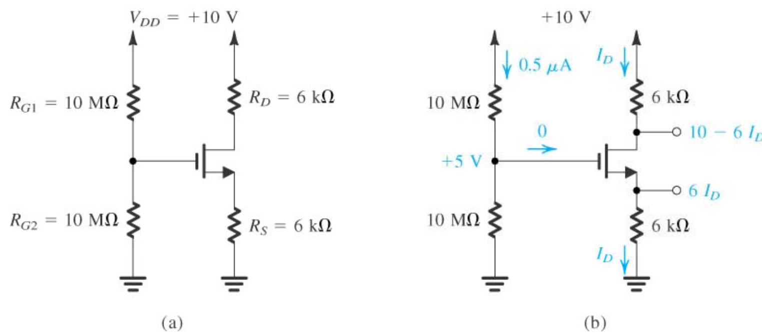
Example 4.5

Analyze the circuit shown in Fig. 4.23(a) to determine the voltages at all nodes and the currents through all branches. Let $V_t = 1$ V and $k_n'(W/L) = 1$ mA/V^2. Neglect the channel-length modulation effect (i.e., assume $\lambda = 0$).



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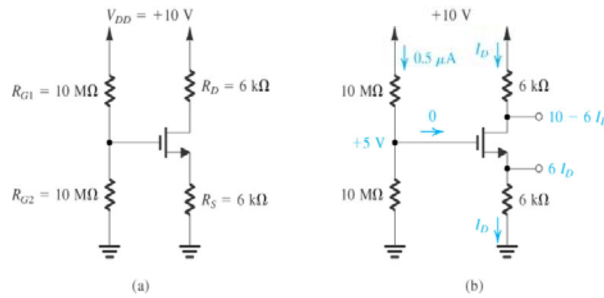
Exercise 4.14 & 4.15

4.14 For the circuit of Fig. 4.23, what is the largest value that R_D can have while the transistor remains in the saturation mode?

Ans. 12 kΩ



D4.15 Redesign the circuit of Fig. 4.23 for the following requirements: V_{DD} = +5 V, I_D = 0.32 mA, V_S = 1.6 V, V_D = 3.4 V, with a 1-μA current through the voltage divider R_{G1}, R_{G2}. Assume the same MOSFET as in Example 4.5.

Ans. R_{G1} = 1.6 MΩ; R_{G2} = 3.4 MΩ, R_S = R_D = 5 kΩ

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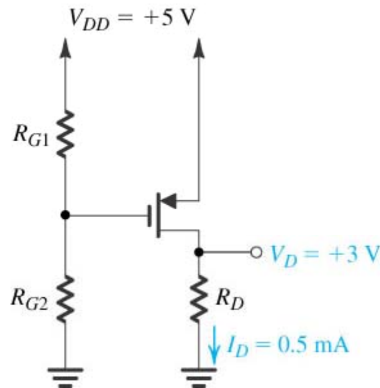
Example 4.6

Design the circuit of Fig. 4.24 so that the transistor operates in saturation with I_D = 0.5 mA and V_D = +3 V. Let the enhancement-type PMOS transistor have V_t = −1 V and $k_p'(W/L) =$ 1 mA/V^2. Assume $\lambda = 0$. What is the largest value that R_D can have while maintaining saturation-region operation?



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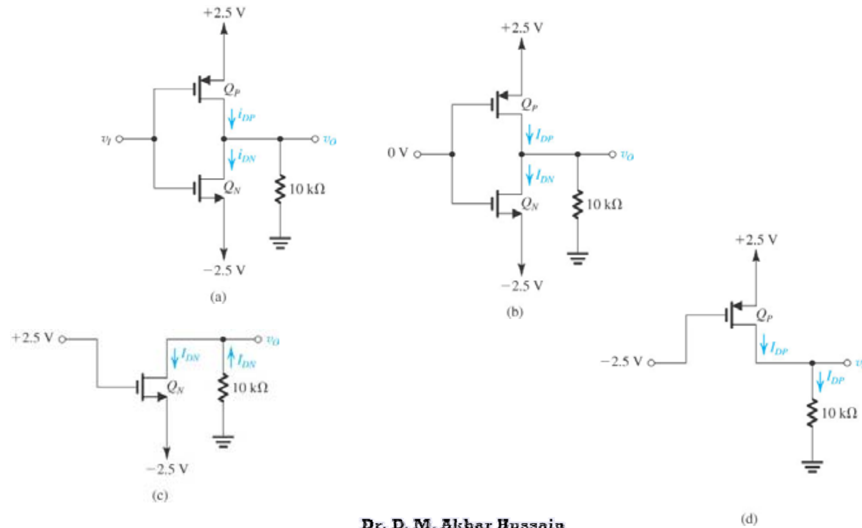
Example 4.7

The NMOS and PMOS transistors in the circuit of Fig. 4.25(a) are matched with $k_n'(W_n/L_n) = k_p'(W_p/L_p) = 1\ \text{mA/V}^2$ and $V_{tn} = -V_{tp} = 1\ \text{V}$. Assuming $\lambda = 0$ for both devices, find the drain currents i_{DN} and i_{DP}, as well as the voltage v_O, for $v_I = 0\ \text{V}$, +2.5 V, and −2.5 V.



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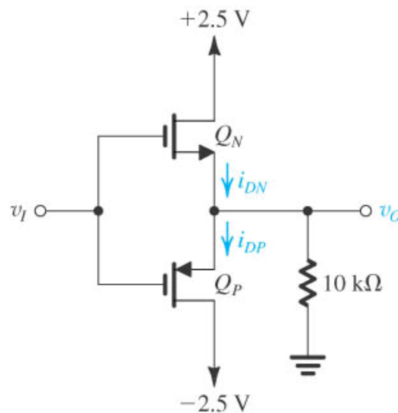
Exercise 4.16

4.16 The NMOS and PMOS transistors in the circuit of Fig. E4.16 are matched with $k_n'(W_n/L_n) = k_p'(W_p/L_p) = 1\ \text{mA/V}^2$ and $V_{tn} = -V_{tp} = 1\ \text{V}$. Assuming $\lambda = 0$ for both devices, find the drain currents i_{DN} and i_{DP} and the voltage v_O for $v_I = 0\ \text{V}$, +2.5 V, and −2.5 V.

Ans. $v_I = 0$ V: 0 mA, 0 mA, 0 V; $v_I = +2.5$ V: 0.104 mA, 0 mA, 1.04 V; $v_I = -2.5$ V: 0 mA, 0.104 mA, −1.04 V



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