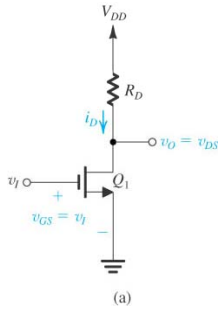
CHAPTER 4

MOS Field-Effect Transistors (MOSFETs)

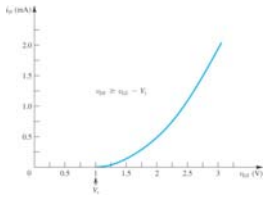
Lecture # 4

MOSFET as an Amplifier



$$v_o = v_{DS} = v_{DD} - R_D i_D$$

$$i_D = \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - v_t)^2$$



Square law expression is non linear between I_D and V_{GS}.

Need to operate in appropriate region for linear behaviour.

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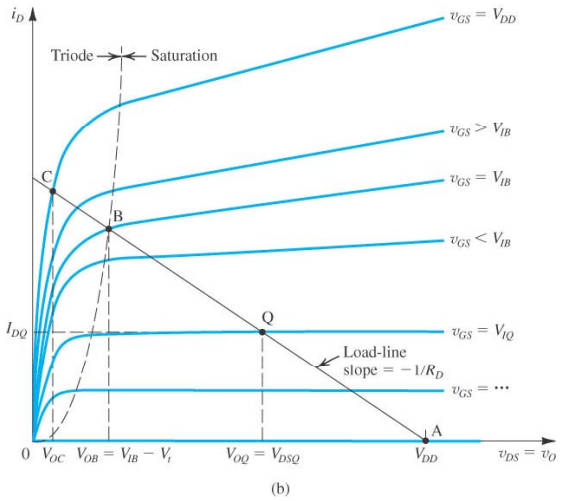
MOSFET as an Amplifier



(b)

$$v_o = v_{DS} = v_{DD} - R_D i_D$$

$$i_D = \frac{v_{DD} - v_{DS}}{R_D}$$

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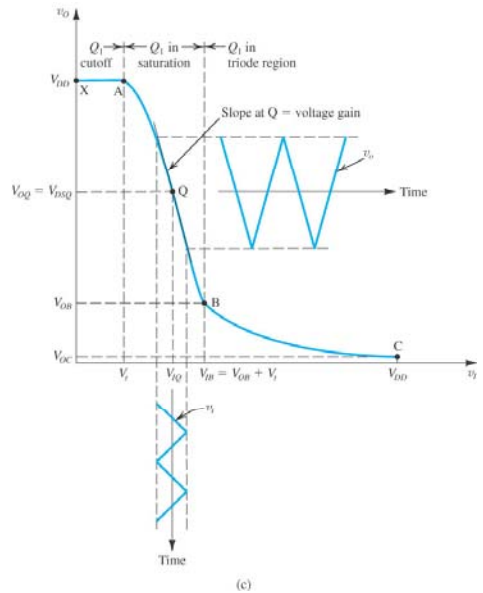
Graphical Derivation of Transfer Characteristics



(c)

$$v_o = v_{DS} = v_{DD} - R_D i_D$$

$$i_D = \frac{v_{DD} - v_{DS}}{R_D}$$

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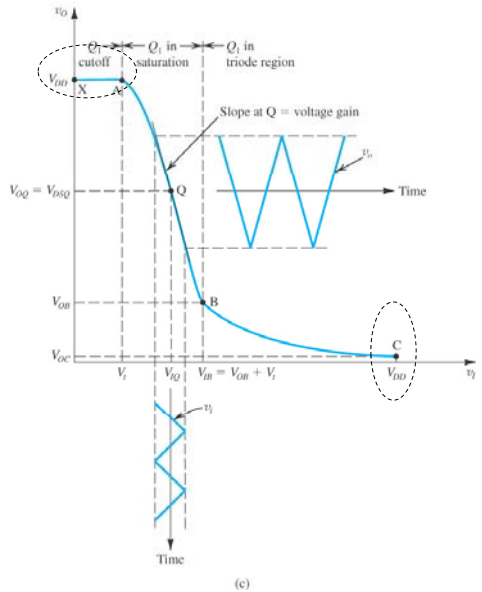
MOSFET as Switch

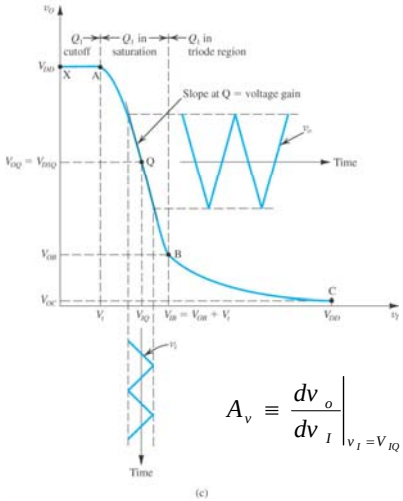
$v_o = v_{DD}$ *off*

$v_o = v_{oc}$ *on*



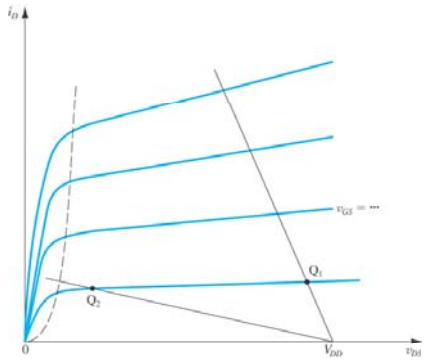
(c)

Selection of Q Point



(c)

$$A_v \equiv \left.\frac{dv_o}{dv_I}\right|_{v_I = V_{IQ}}$$



It is very important to note that the selection of Q point should be made in such a way that the signal is not distorted/clipped, we can see that if the Q point is near V_{DD} the output will be clipped off and if it is close to triode boundary signal will be distorted. So basically, the Q point should be lower than V_{DD} and higher than V_{DSQ} to have maximum swing.

However, one should note that selection of Q point is dependent on what you select the load resistor, which determines the transfer characteristics.

Analysis: MOSFET as a Linear Amplifier

Cutoff Segment X - A, $v_I \le v_t \quad v_o = V_{DD}$

Saturation Segment A - Q - B $v_I \ge v_t \quad v_o \ge v_I - V_t$

$i_D = \frac{1}{2}\mu_n c_{ox}\frac{W}{L}(v_I - V_t)^2$ and $v_o = V_{DD} - R_D i_D$ from these two equations

we get $v_O = v_{DD} - \frac{1}{2}R_D\mu_n c_{ox}\frac{W}{L}(v_I - V_t)^2$

we can determine gain $A_v = \left.\frac{dv_o}{dv_I}\right|_{v_I = V_{IQ}} = -R_D\mu_n c_{ox}\frac{W}{L}(V_{IQ} - V_t)$

using the above two equation and substituting

$v_I = V_{IQ} \quad v_o = V_{OQ}$

$V_{IQ} - V_t = V_{OV}$

$A_v = \frac{2(V_{DD} - V_{OQ})}{V_{OV}} = \frac{2V_{RD}}{V_{OV}}$ where $(V_{RD} = V_{DD} - V_{OQ})$

Triode Segment B - C $v_I \ge V_t \quad v_o \le v_I - V_t$

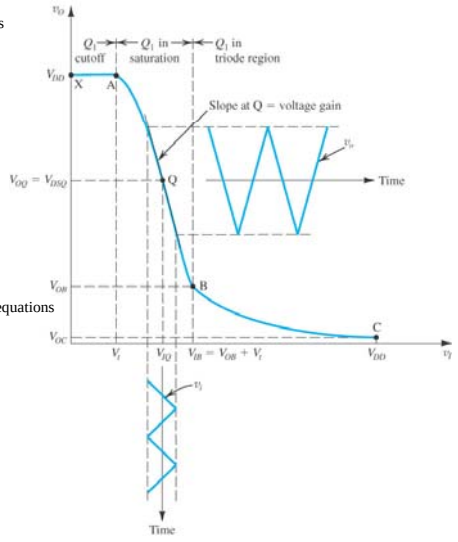
$i_D = \mu_n c_{ox}\frac{W}{L}\left[(v_I - V_t)v_O - \frac{1}{2}v_O^2\right]$ and $v_o = V_{DD} - R_D i_D$ from these two equations

we get $v_O = V_{DD}\Big/\left[1 + R_D\mu_n c_{ox}\frac{W}{L}(v_I - V_t)\right]$ Reference 4.43 Equation

we know $r_{DS} = \frac{1}{\left[\mu_n c_{ox}\frac{W}{L}(v_I - V_t)\right]}$

$v_O = \frac{V_{DD}}{1 + R_D\frac{1}{r_{DS}}} = V_{DD}\frac{r_{DS}}{r_{DS} + R_D}$ Usually $r_{DS} << R_D$

$v_O \cong V_{DD}\frac{r_{DS}}{R_D}$



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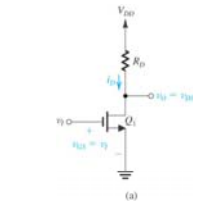
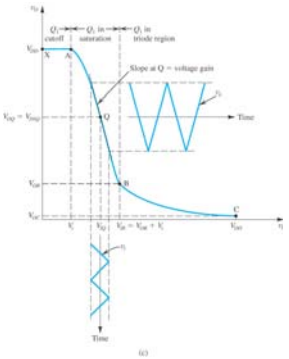
Example 4.8





Point X : $v_I = 0v \quad v_O = 10v$ Point A : $v_I = 1v \quad v_O = 10v$

Point B : $v_I = V_{IB} = V_{OB} + V_t = V_{OB} + 1$

As we are in the saturation region so $v_O = V_{DD} - \frac{1}{2}R_D\mu_n c_{ox}\frac{W}{L}(v_I - V_t)^2$

we substitude above as $v_O = V_{OB}$ so $V_{OB} = 10 - \frac{1}{2}R_D\mu_n c_{ox}\frac{W}{L}(V_{OB} + 1 - 1)^2$

$9V_{OB}^2 + V_{OB} - 10 = 0$ It has two roots and possible one is $V_{OB} = 1v$

Therefore $V_{IB} = V_{OB} + V_t = 1 + 1 = 2v$

Point C : $v_O = \frac{V_{DD}}{\left[1 + R_D\mu_n c_{ox}\frac{W}{L}(v_I - V_t)\right]}$ Reference 4.43 Equation

$= 10/1 + 18 \times 1 \times (10 - 1) = 0.061$

Next is the biasing the amplifier, since the segment extends from 1 volt to 10 volt may be we select the Q point at 4 v.

so the current $I_D = \frac{V_{DD} - V_{OQ}}{R_D} = \frac{10 - 4}{18} = 0.333mA$

we can calculate over drive voltage $I_D = \frac{1}{2}k_n'\frac{W}{L}V_{OV}^2$

$V_{OV} = \sqrt{\frac{2 \times 0.333}{1}} = 0.816v$

So we operate MOSFET at a dc gate to source voltage $= V_{GSQ} = V_t + V_{OV} = 1.816v$

Volatge gain from 4.40 $A_v = -18 \times 1 \times (1.816 - 1) = -14.7v/v$

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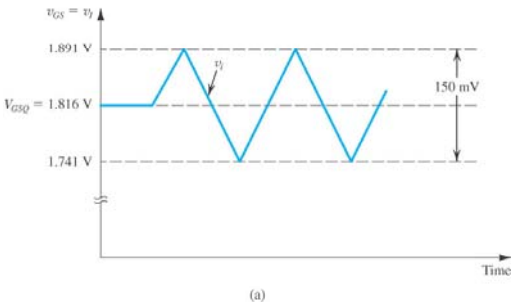
Example 4.8

Superimpose the following signal at 1.816 v (Q point)



(a)

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v_{GS} - v_t)^2$$

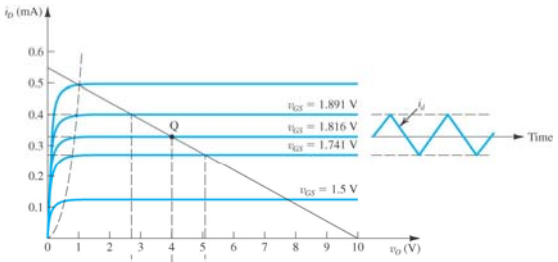
So at $v_{GS} = 1.741\,\text{v}, i_D = \frac{1}{2}\times 1\times(1.741-1)^2 = 0.275mA$

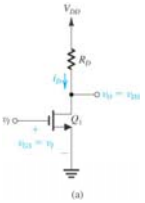
At $v_{GS} = 1.816\,\text{v}, i_D = \frac{1}{2}\times 1\times(1.816-1)^2 = 0.333mA$

At $v_{GS} = 1.891\,\text{v}, i_D = \frac{1}{2}\times 1\times(1.891-1)^2 = 0.397mA$

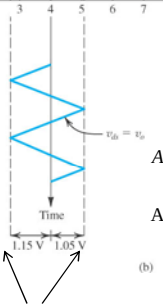
Look at the +ve & -ve increment in the drain current, are they same ?

Example 4.8





(a)



(b)

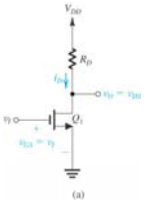
The output will vary around bias value of V_{OQ} = 4 V

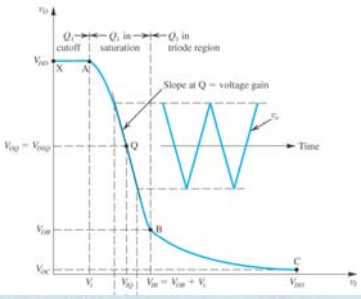
At $v_{GS} = 1.741\,\text{v}, i_D = 0.275mA$ and $v_o = v_{DD} - i_D R_D = 10 - 0.275\times 18 = 5.05v$

At $v_{GS} = 1.891\,\text{v}, i_D = 0.397mA$ and $v_o = v_{DD} - i_D R_D = 10 - 0.397\times 18 = 2.85v$

Look at the output for +ve and –ve excursions ?

Exercise 4.17 & 4.18





4.17 For the circuit studied in Example 4.8 above and with reference to the transfer characteristic sketched in Fig. 4.26(c): (a) Give the values of V_{IQ}, V_{IB}, V_{OQ}, and V_{OB}. (b) Use the values in (a) to determine the largest allowable value of the negative peak of the output signal and the magnitude of the corresponding positive peak of the input signal. Disregard distortion caused by the square-law MOSFET characteristic. (c) Repeat (b) for the positive-output peak and the corresponding negative-input peak. (d) From the results of (b) and (c), what is the maximum amplitude of a sine wave that can be applied at the input and the corresponding output amplitude. What value of gain do these amplitudes imply? Why is it different from the 14.7 V/V found in Example 4.8?

Ans. (a) 1.816 V, 2 V, 4 V, 1 V; (b) 3 V, 0.184 V; (c) 6 V, 0.816 V; (d) 0.184 V, 3 V, 16.3 V/V, because of the nonlinear transfer characteristic.

4.18 Derive the voltage-gain expression in Eq. (4.41). Use the expression to verify the gain value found in Example 4.8.

$$A_v = \frac{2V_{RD}}{V_{OV}}$$

$$V_O = V_{DD} - R_D I_D \qquad \{v_I = V_{IQ}, V_O = V_{OQ}, V_{OV} = V_{IQ} - V_t\}$$

$$I_D = \frac{1}{2} K_n' \frac{W}{L}(v_I - V_t)^2$$

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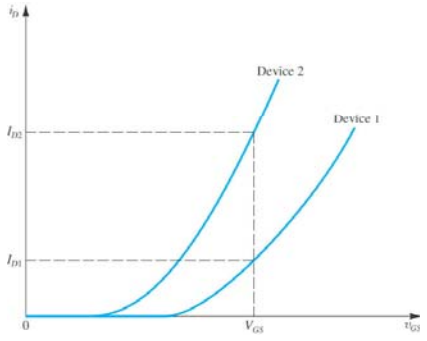
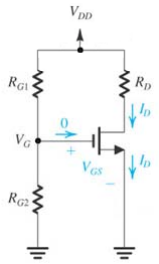
Biasing MOS Amplifier Circuits



Not a good idea for biasing MOSFET ?



$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$

The use of fixed bias (constant V_{GS}) can result in a large variability in the value of I_D. Devices 1 and 2 represent extremes among units of the same type.

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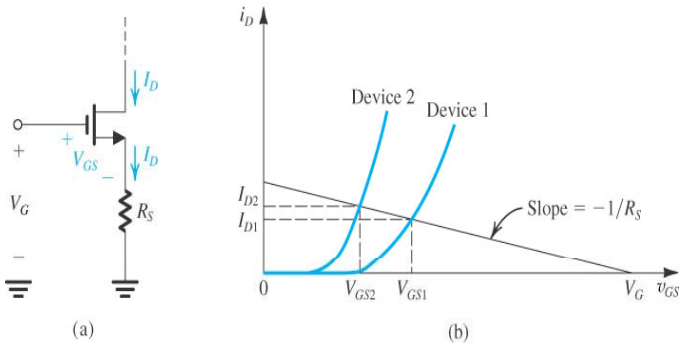
Biasing with fixed gate voltage V_G & having a source resistor R_S

$$V_G = V_{GS} + R_S I_D$$

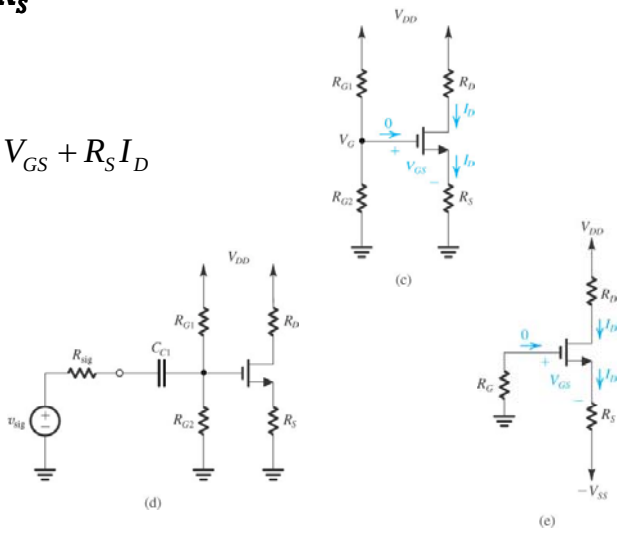


(a) Basic Arrangement

(b) Reduced variability in I_D

Biasing with fixed gate voltage V_G & having a source resistor R_S

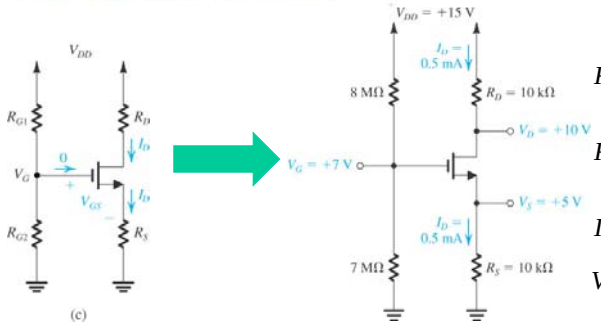
$$V_G = V_{GS} + R_S I_D$$



(c) Practical implementation using a single supply; **(d)** Coupling of a signal source to the gate using a capacitor C_{C1}; **(e)** Practical implementation using two supplies.

Example 4.9

It is required to design the circuit of Fig. 4.30(c) to establish a dc drain current $I_D = 0.5$ mA. The MOSFET is specified to have $V_t = 1$ V and $k_n'W/L = 1$ mA/V^2. For simplicity, neglect the channel-length modulation effect (i.e., assume $\lambda = 0$). Use a power-supply $V_{DD} = 15$ V. Calculate the percentage change in the value of I_D obtained when the MOSFET is replaced with another unit having the same $k_n'W/L$ but $V_t = 1.5$ V.



$$R_D = \frac{V_{DD} - V_D}{I_D}$$

$$R_S = \frac{V_S}{I_D}$$

$$I_D = \frac{1}{2} K_n' \frac{W}{L} V_{OV}^2$$

$$V_{GS} = V_t + V_{OV} \qquad V_G = V_S + V_{GS}$$

As a rule of thumb for classical biasing we select R_D and R_S in such a way that the V_{DD} voltage is divided equally across R_D , MOSFET (Drain to Source) & R_S , which means one third across these three components.

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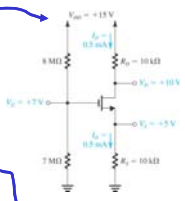
Exercise 4.19 & 4.20

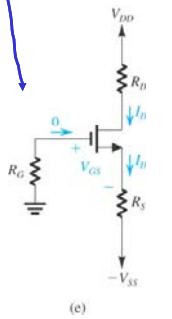
4.19 Consider the MOSFET in Example 4.9 when fixed-V_{GS} bias is used. Find the required value of V_{GS} to establish a dc bias current $I_D = 0.5$ mA. Recall that the device parameters are $V_t = 1$ V, $k_n'W/L = 1$ mA/V^2, and $\lambda = 0$. What is the percentage change in I_D obtained when the transistor is replaced with another having $V_t = 1.5$ V?

Ans. $V_{GS} = 2$ V; −75%

D4.20 Design the circuit of Fig. 4.30(e) to operate at a dc drain current of 0.5 mA and $V_D = +2$ V. Let $V_t = 1$ V, $k_n'W/L = 1$ mA/V^2, $\lambda = 0$, $V_{DD} = V_{SS} = 5$ V. Use standard 5% resistor values (see Appendix G), and give the resulting values of I_D, V_D, and V_S.

Ans. $R_D = R_S = 6.2$ kΩ; $I_D = 0.49$ mA, $V_S = -1.96$ V, and $V_D = +1.96$ V. R_G can be selected in the range of 1 MΩ to 10 MΩ.





First find R_D and then over voltage V_{OV}, then find V_S, once you have V_S find R_S.

Now calculate new I_D by substituting $V_{GS} = -V_S = V_{SS} - R_S I_D$

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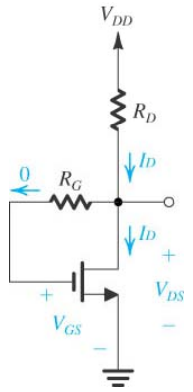
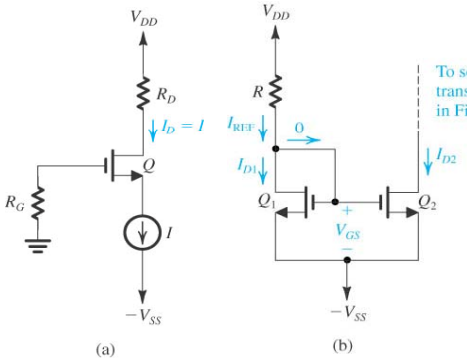
Biasing: Drain-to-Gate Feedback Resistor

$$V_{GS} = V_{DS} = V_{DD} - R_D I_D$$

$$V_{DD} = V_{GS} + R_D I_D$$



Biasing Using a Constant Current Source



$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (v_{GS} - v_t)^2$$

$$I_{D1} = I_{REF} = \frac{v_{DD} + v_{SS} - v_{GS}}{R}$$

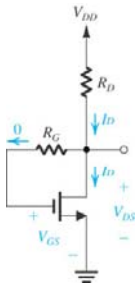
$$I = I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (v_{GS} - v_t)^2$$

$$I = I_{REF}\frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}$$

Exercise 4.21 & 4.22

D4.21 It is required to design the circuit in Fig. 4.32 to operate at a dc drain current of 0.5 mA. Assume V_{DD} = +5 V, $k_n'W/L$ = 1 mA/V^2, V_t = 1 V, and λ = 0. Use a standard 5% resistance value for R_D, and give the actual values obtained for I_D and V_D.

Ans. R_D = 6.2 kΩ; $I_D \cong$ 0.49 mA; $V_D \cong$ 1.96 V

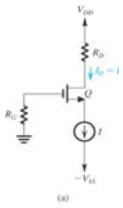


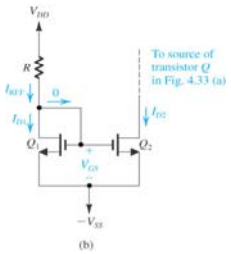
First find V_{OV} and then V_{GS}, for this configuration $V_{GS} = V_{DS}$, find R_D.

Now calculate new I_D by substituting $V_{GS} = V_D = V_{DD} - R_D I_D$

D4.22 Using two transistors Q_1 and Q_2 having equal lengths but widths related by W_2/W_1 = 5, design the circuit of Fig. 4.33(b) to obtain I = 0.5 mA. Let $V_{DD} = -V_{SS}$ = 5 V, $k_n'(W/L)_1$ = 0.8 mA/V^2, V_t = 1 V, and λ = 0. Find the required value for R. What is the voltage at the gates of Q_1 and Q_2? What is the lowest voltage allowed at the drain of Q_2 while Q_2 remains in the saturation region?

Ans. 85 kΩ; −3.5 V; −4.5 V





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