# BJT as an Amplifier & a Switch, Large Signal Operation, Graphical Analysis, BJT at DC, Biasing BJT, Small Signal Operation Model, Hybrid Pi-Model, T Model.

**Lecture # 7**

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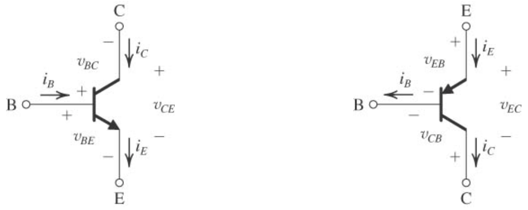
## Direction of Current Flow & Operation for Amplifier Application



$v_{BE} > V_{BEon}; V_{BEon} \cong 0.5V$ Typically, $v_{BE} = 0.7V$

$v_{BC} \geq V_{BC0n}; V_{BCon} \cong 0.4V$ Typically, $v_{CE} \geq 0.3V$

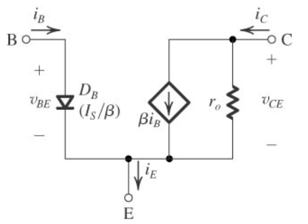
$i_C = I_S e^{v_{BE}/V_T}$

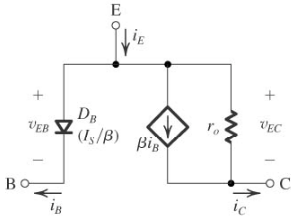
$v_{EB} > V_{EBon}; V_{EBon} \cong 0.5V$ Typically, $v_{EB} = 0.7V$

$v_{CB} \geq V_{CB0n}; V_{CBon} \cong 0.4V$ Typically, $v_{EC} \geq 0.3V$

$i_C = I_S e^{v_{EB}/V_T}$

# Large Signal Equivalent Model





$$i_B = \frac{I_S}{\beta} e^{v_{BE}/V_T}$$

$$i_B = \frac{I_S}{\beta} e^{v_{EB}/V_T}$$

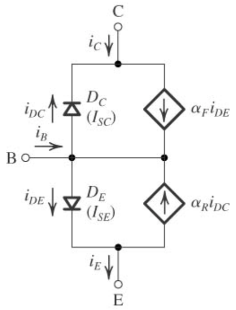
$$i_C = I_S e^{v_{BE}/V_T}\left(1 + \frac{v_{CE}}{V_A}\right)$$

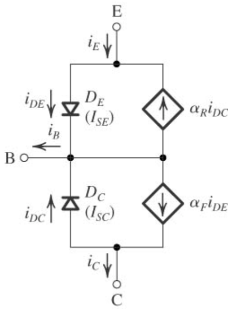
$$i_C = I_S e^{v_{EB}/V_T}\left(1 + \frac{v_{EC}}{|V_A|}\right)$$

$$r_O = \frac{V_A}{I_S e^{v_{BE}/V_T}}$$

$$r_O = \frac{|V_A|}{I_S e^{v_{EB}/V_T}}$$

# Ebers-Moll Model





$$i_{DE} = I_{SE}(e^{v_{BE}/V_T} - 1)$$

$$i_{DE} = I_{SE}(e^{v_{EB}/V_T} - 1)$$

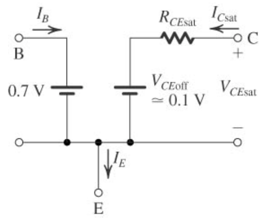
$$i_{DC} = I_{SC}(e^{v_{BC}/V_T} - 1)$$

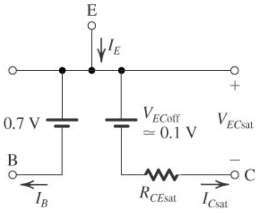
$$i_{DC} = I_{SC}(e^{v_{CB}/V_T} - 1)$$

$$\alpha_F I_{SE} = \alpha_R I_{SC} = I_S$$

$$\frac{I_{SC}}{I_{SE}} = \frac{\alpha_F}{\alpha_R} = \frac{CBJ \text{ Area}}{EBJ \text{ Area}}$$

# Operation in Saturation Mode





$v_{BE} > V_{BEon}; V_{BEon} \cong 0.5V$  Typically, $v_{BE} = 0.7V - 0.8V$

$v_{BC} \geq V_{BC0n}; V_{BCon} \cong 0.4V$  Typically, $v_{BC} = 0.5V - 0.6V$

$v_{CE} = V_{CEsat} = 0.1V - 0.2V$

$v_{EB} > V_{EBon}; V_{EBon} \cong 0.5V$  Typically, $v_{EB} = 0.7V - 0.8V$

$v_{CB} \geq V_{CB0n}; V_{CBon} \cong 0.4V$  Typically, $v_{CB} = 0.5V - 0.6V$

$v_{CE} = V_{CEsat} = 0.1V - 0.2V$

$$I_{Csat} = \beta_{forced} I_B$$

$$\beta_{forced} \leq \beta_F$$

Beta forced means that the transistor is operating in saturated mode. The ratio of Beta forward and the forced beta is called **overdrive factor**, the more transistor goes into saturation the voltage $V_{CE}$ will also be lower.

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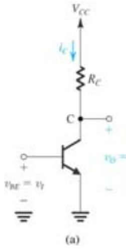
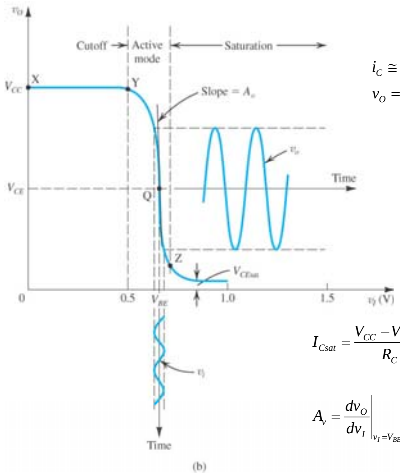
# Transfer Characteristics of CE Amplifier



$$v_O = v_{CE} = V_{CC} - R_C i_C$$



$$i_C \cong I_S e^{v_{BE}/V_T} = I_S e^{v_I/V_T}$$
$$v_O = v_{CE} = V_{CC} - R_C I_S e^{v_I/V_T}$$

The resistance $R_C$ has two functions, firstly, to establish the desired DC bias voltage at the collector and second converting the current signal into voltage.

$$I_{Csat} = \frac{V_{CC} - V_{CEsat}}{R_C}$$

$$A_v = \left. \frac{dv_O}{dv_I} \right|_{v_I = V_{BE}}$$

$$A_v = \frac{V_{CC} - V_{CE}}{V_T}$$

**(a)** Basic common-emitter amplifier circuit. **(b)** Transfer characteristic of the circuit in (a). The amplifier is biased at a point Q, and a small voltage signal $v_i$ is superimposed on the dc bias voltage $V_{BE}$. The resulting output signal $v_o$ appears superimposed on the dc collector voltage $V_{CE}$. The amplitude of $v_o$ is larger than that of $v_i$ by the voltage gain $A_v$.

# Example 5.2

Consider a common-emitter circuit using a BJT having $I_S = 10^{-15}$ A, a collector resistance $R_C = 6.8\ \text{k}\Omega$, and a power supply $V_{CC} = 10$ V.

(a) Determine the value of the bias voltage $V_{BE}$ required to operate the transistor at $V_{CE} = 3.2$ V. What is the corresponding value of $I_C$?

(b) Find the voltage gain $A_v$ at this bias point. If an input sine-wave signal of 5-mV peak amplitude is superimposed on $V_{BE}$, find the amplitude of the output sine-wave signal (assume linear operation).

(c) Find the positive increment in $v_{BE}$ (above $V_{BE}$) that drives the transistor to the edge of saturation, where $v_{CE} = 0.3$ V.

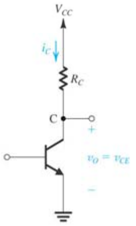
(d) Find the negative increment in $v_{BE}$ that drives the transistor to within 1% of cutoff (i.e., to $v_O = 0.99V_{CC}$).

$I_C = 1$ mA
$V_{BE} = 0.6908$ V
$A_v = -272$ V/V
$V_o = 1.36$ V
$\Delta V_{BE} = 12$ mV
$\Delta V_{BE} = -105.5$ mV

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

$$A_v = \frac{V_{CC} - V_{CE}}{V_T}, \hat{V}_0 = A_v V_i$$

$$\Delta v_{BE} = ?$$



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# Exercise 5.19

**5.19** For the situation described in Example 5.2, while keeping $I_C$ unchanged at 1 mA, find the value of $R_C$ that will result in a voltage gain of −320 V/V. What is the largest negative signal swing allowed at the output (assume that $v_{CE}$ is not to decrease below 0.3 V)? What (approximately) is the corresponding input signal amplitude? (Assume linear operation).

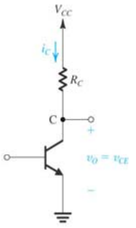
**Ans.** 8 kΩ; 1.7 V; 5.3 mV

$$A_v = -\frac{I_C R_C}{V_T}$$

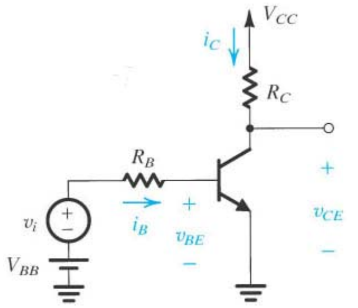
$$V_C = V_{CC} - I_C R_C$$

$$Negative - Swing = V_{CE} - V_C$$

$$Input - Amplitude = \frac{V_{CE} - V_C}{A_v}$$



# Graphical Analysis



$$v_{CE} = V_{CC} - i_C R_C$$

$$i_C = \frac{V_{CC}}{R_C} - \frac{1}{R_C} v_{CE}$$ this shows a lineae relationship between $v_{CE}$ & $i_C$.

This linear relationship can be represented by a straight line.

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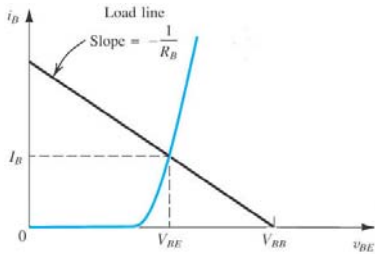
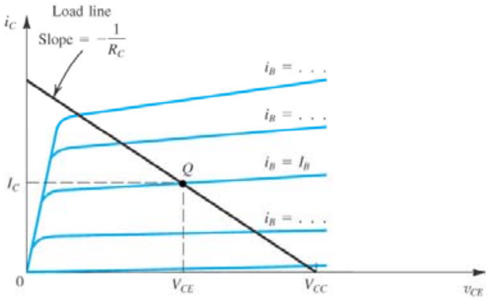
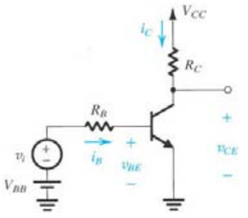
# Graphical Analysis



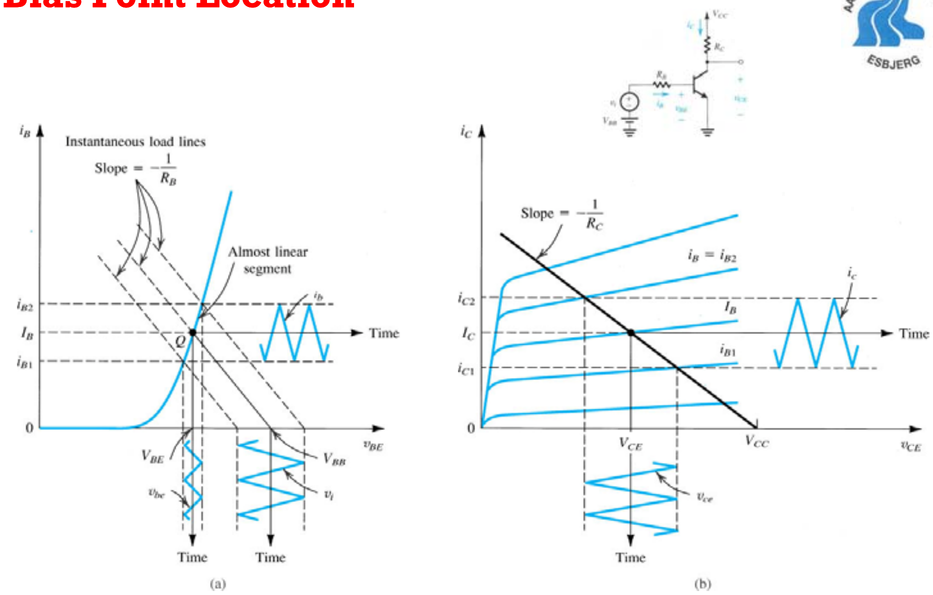


$$v_{BE} = V_{BB} + i_B R_B$$
$$V_{BB} = v_{BE} - i_B R_B$$



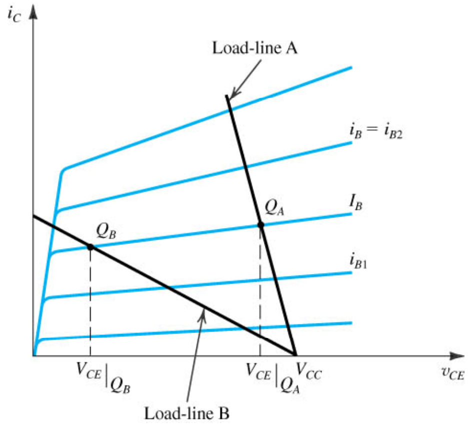
$$v_{CE} = V_{CC} - i_C R_C$$
$$i_C = \frac{V_{CC}}{R_C} - \frac{1}{R_C} v_{CE}$$

# Bias Point Location



Graphical determination of the signal components $v_{be}$, $i_b$, $i_c$, and $v_{ce}$ when a signal component $v_i$ is superimposed on the dc voltage $V_{BB}$ (see Fig. above).

# Bias Point Location

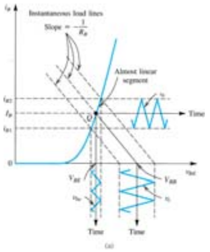


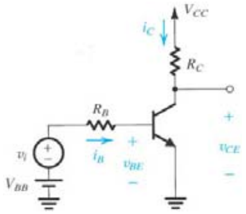
Effect of bias-point location on allowable signal swing: Load-line A results in bias point $Q_A$ with a corresponding $V_{CE}$ which is too close to $V_{CC}$ and thus limits the positive swing of $v_{CE}$. At the other extreme, load-line B results in an operating point too close to the saturation region, thus limiting the negative swing of $v_{CE}$.

# Exercise 5.20

**5.20** Consider the circuit of Fig. 5.27 with $V_{BB} = 1.7$ V, $R_B = 100$ kΩ, $V_{CC} = 10$ V, and $R_C = 5$ kΩ. Let the transistor $\beta = 100$. The input signal $v_i$ is a triangular wave of 0.4 V peak-to-peak. Refer to Fig. 5.30, and use the geometry of the graphical construction shown there to answer the following questions: (a) If $V_{BE} = 0.7$ V, find $I_B$. (b) Assuming operation on a straight line segment of the exponential $i_B$–$v_{BE}$ curve, show that the inverse of its slope is $V_T/I_B$, and compute its value. (c) Find approximate values for the peak-to-peak amplitude of $i_b$ and of $v_{be}$. (d) Assuming the $i_C$–$v_{CE}$ curves to be horizontal (i.e., ignoring the Early effect), find $I_C$ and $V_{CE}$. (e) Find the peak-to-peak amplitude of $i_c$ and of $v_{ce}$. (f) What is the voltage gain of this amplifier?

**Ans.** (a) 10 μA; (b) 2.5 kΩ; (c) 4 μA, 10 mV; (d) 1 mA, 5 V; (e) 0.4 mA, 2 V; (f) −5 V/V





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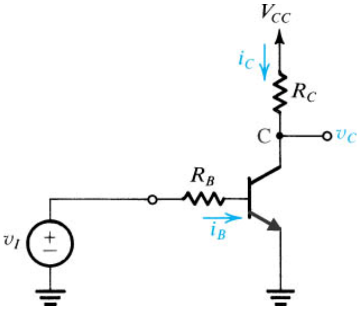
# Operation as a Switch

To use it as switch we utilize the cutoff and saturation modes of operations. A simple circuit used to illustrate the different modes of operations of the BJT.



$$i_B = \frac{v_i - V_{BE}}{R_B} \;,\; i_C = \beta\, i_B$$

$v_C > v_B - 0.4$ so CBJ is reversed biased as long as this holds.

$$v_C = V_{CC} - R_C i_C$$

$I_{C(EOS)} = \dfrac{V_{CC} - 0.3}{R_C}$ Edge of saturation

$I_{B(EOS)} = \dfrac{I_{C(EOS)}}{\beta}$ when we assume $v_{BE} = 0.7V$

$V_{I(EOS)} = I_{B(EOS)} R_B + V_{BE}$ (where vi drives the BJT to edge of saturation).

Increasing $v_i$ beyond $V_{I(EOS)}$ increase the base current which send BJT deeper into saturation but $V_{CE}$ only change slightly, as

$$I_{Csat} = \frac{V_{CC} - V_{CEsat}}{R_C}$$

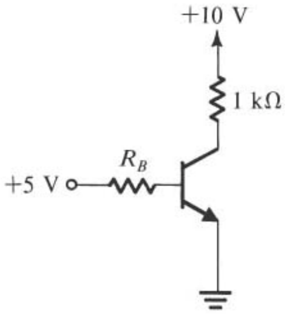
It should be noted that in saturation one can force BJT to operate at desired $\beta$, which is called $\beta_{\text{forced}}$.

$$\beta_{\text{forced}} \equiv \frac{I_{Csat}}{I_B}$$

$$\frac{I_B}{I_{B(EOS)}} = over - drive - factor$$

# Example 5.3

The transistor in Fig. 5.33 is specified to have $\beta$ in the range of 50 to 150. Find the value of $R_B$ that results in saturation with an overdrive factor of at least 10.



$$V_C = V_{CEsat} \approx 0.2V$$

$$I_{Csat} = \frac{V_{CC} - V_{CEsat}}{R_C}$$

$$I_{B(EOS)} = \frac{I_{Csat}}{\beta_{\min}}$$

$$\frac{I_B}{I_{B(EOS)}} = over - drive - \ factor$$

$$R_B = \frac{V_B - v_{BE}}{I_B}$$

$I_{C(sat)} = 9.8$ mA
$I_{B(EOS)} = 0.196$ mA
$I_B = 1.96$ mA
$R_B = 2.2$ K

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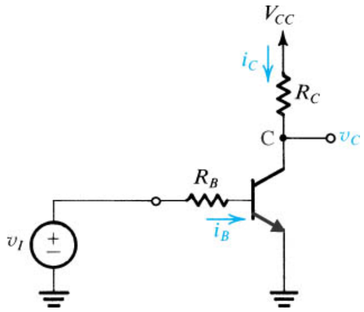
# Exercise 5.21

**5.21** Consider the circuit in Fig. 5.32 for the case $V_{CC} = +5$ V, $v_I = +5$ V, $R_B = R_C = 1$ kΩ, and $\beta = 100$. Calculate the base current, the collector current, and the collector voltage. If the transistor is saturated, find $\beta_{\text{forced}}$. What value should $R_B$ be raised to in order to bring the transistor to the edge of saturation?

**Ans.** 4.3 mA; 4.8 mA; 0.2 V; 1.1; 91.5 kΩ



# Example 5.4

Consider the circuit shown in Fig. 5.34(a), which is redrawn in Fig. 5.34(b) to remind the reader of the convention employed throughout this book for indicating connections to dc sources. We wish to analyze this circuit to determine all node voltages and branch currents. We will assume that $\beta$ is specified to be 100.

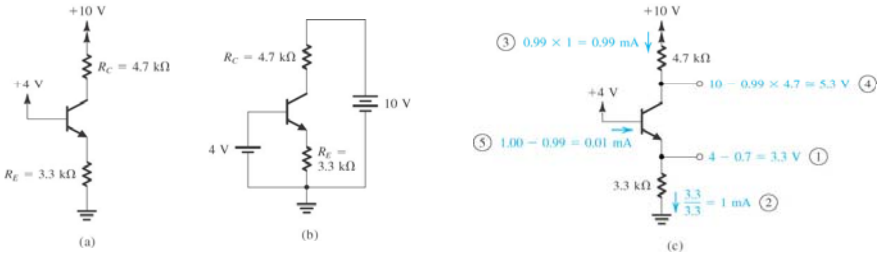
$$V_E = V_B - V_{BE}$$

$$I_E = \frac{V_E - 0}{R_E}$$

$$I_C = \alpha I_E \qquad \alpha = \frac{\beta}{\beta + 1}$$

$$V_C = V_{CC} - I_C R_C$$

$$I_B = \frac{I_E}{\beta + 1}$$



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# Example 5.5

We wish to analyze the circuit of Fig. 5.35(a) to determine the voltages at all nodes and the currents through all branches. Note that this circuit is identical to that of Fig. 5.34 except that the voltage at the base is now +6 V. Assume that the transistor $\beta$ is specified to be *at least* 50.

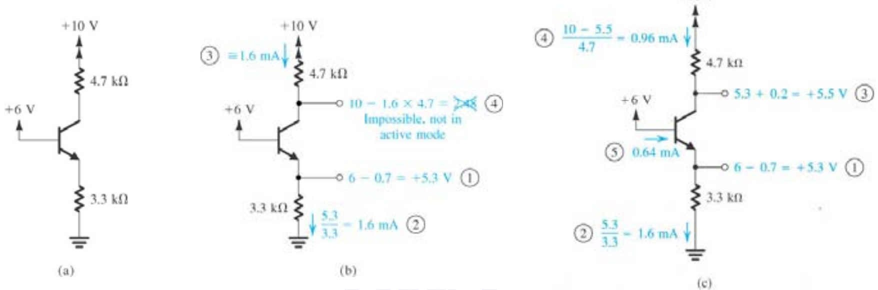
$$V_E = V_B - V_{BE}$$

$$I_E = \frac{V_E - 0}{R_E}$$

$$I_C = \alpha I_E \qquad \alpha = \frac{\beta}{\beta + 1}$$

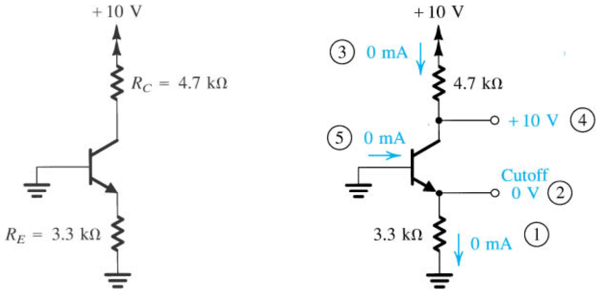
$$V_C = V_{CC} - I_C R_C$$

$$I_B = \frac{I_E}{\beta + 1}$$



# Example 5.6

We wish to analyze the circuit in Fig. 5.36(a) to determine the voltages at all nodes and the currents through all branches. Note that this circuit is identical to that considered in Examples 5.4 and 5.5 except that now the base voltage is zero.



(a) (b)

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# Exercises 5.22, 5.23 & 5.24

**D5.22** For the circuit in Fig. 5.34(a), find the highest voltage to which the base can be raised while the transistor remains in the active mode. Assume $\alpha \simeq 1$.

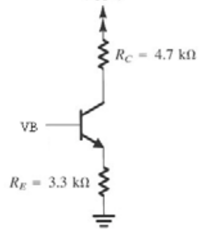
**Ans.** +4.7 V

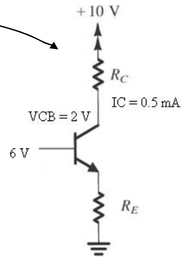
**D5.23** Redesign the circuit of Fig. 5.34(a) (i.e., find new values for $R_E$ and $R_C$) to establish a collector current of 0.5 mA and a reverse-bias voltage on the collector–base junction of 2 V. Assume $\alpha \simeq 1$.

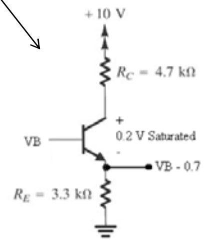
**Ans.** $R_E$ = 6.6 kΩ; $R_C$ = 8 kΩ

**5.24** For the circuit in Fig. 5.35(a), find the value to which the base voltage should be changed to so that the transistor operates in saturation with a forced $\beta$ of 5.

**Ans.** +5.18 V







# Example 5.7

We desire to analyze the circuit of Fig. 5.37(a) to determine the voltages at all nodes and the currents through all branches.

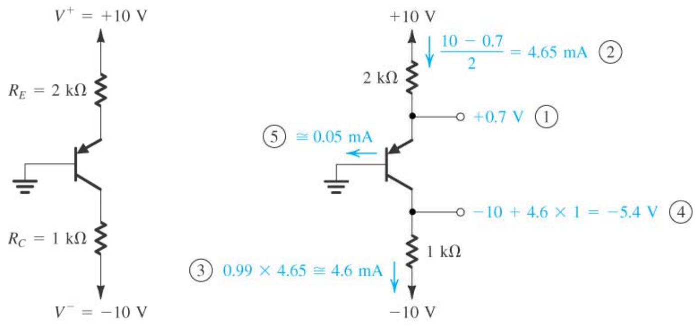
$$V_E = V_B - V_{BE}$$

$$I_E = \frac{V_E - 0}{R_E}$$

$$I_C = \alpha I_E \qquad \alpha = \frac{\beta}{\beta + 1}$$

$$V_C = V_{CC} - I_C R_C$$

$$I_B = \frac{I_E}{\beta + 1}$$



(a) (b)

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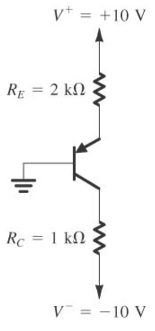
# Exercises 5.25 & 5.26

**D5.25** For the circuit in Fig. 5.37(a), find the largest value to which $R_C$ can be raised while the transistor remains in the active mode.

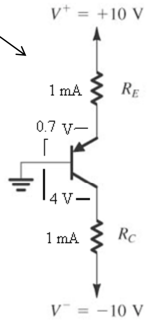
**Ans.** 2.26 kΩ

**D5.26** Redesign the circuit of Fig. 5.37(a) (i.e., find new values for $R_E$ and $R_C$) to establish a collector current of 1 mA and a reverse bias on the collector–base junction of 4 V. Assume $\alpha \simeq 1$.

**Ans.** $R_E = 9.3$ kΩ; $R_C = 6$ kΩ



(a)



# Example 5.8

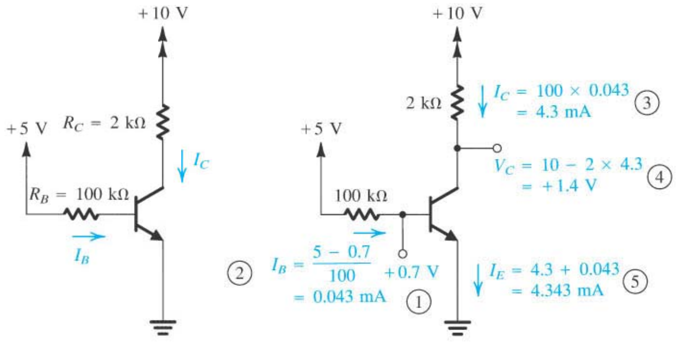
We want to analyze the circuit in Fig. 5.38(a) to determine the voltages at all nodes and the currents in all branches. Assume $\beta = 100$.

$$I_B = \frac{V_B - V_{BE}}{R_B}$$

$$I_C = \beta I_B$$

$$V_C = V_{CC} - I_C R_C$$

$$I_E = I_B + I_C$$

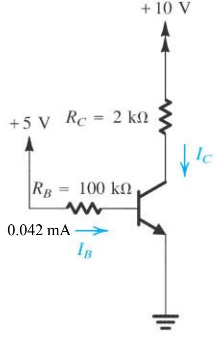


(a) (b)

# Exercises 5.27

**D5.27** The circuit of Fig. 5.38(a) is to be fabricated using a transistor type whose $\beta$ is specified to be in the range of 50 to 150. That is, individual units of this same transistor type can have $\beta$ values anywhere in this range. Redesign the circuit by selecting a new value for $R_C$ so that all fabricated circuits are guaranteed to be in the active mode. What is the range of collector voltages that the fabricated circuits may exhibit?

**Ans.** $R_C = 1.5\ \text{k}\Omega$; $V_C = 0.3$ V to 6.8 V



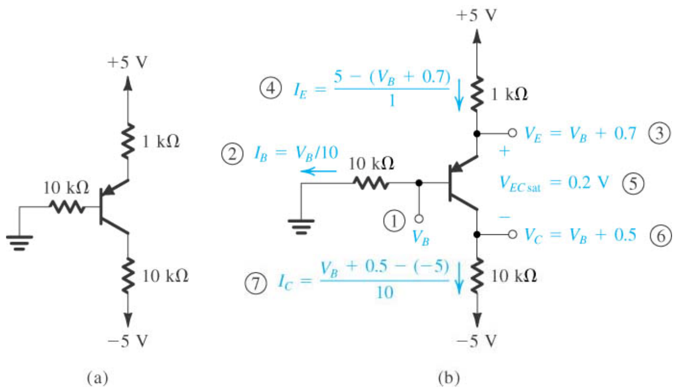
(a)

$$R_C = \frac{V_{CC} - V_C}{i_B \beta}$$

$$Range - of - V_C = 0.3 - - - - - (V_C - i_C R_C)$$

# Example 5.9

We want to analyze the circuit of Fig. 5.39 to determine the voltages at all nodes and the currents through all branches. The minimum value of $\beta$ is specified to be 30.



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# Example 5.10

We want to analyze the circuit of Fig. 5.40(a) to determine the voltages at all nodes and the currents through all branches. Assume $\beta = 100$.

$$V_{BB} = \frac{V_{CC}}{R_{B1}+R_{B2}} R_{B2}$$

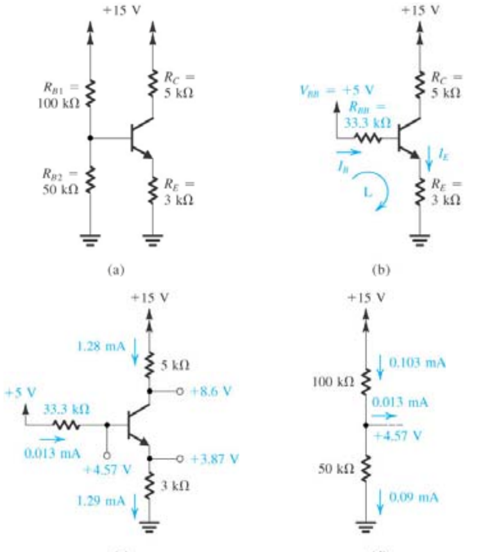
$$R_{BB} = (R_{B1} \parallel R_{B2})$$

$$V_{BB} = I_B R_{BB} + V_{BE} + I_E R_E$$

$$I_B = \frac{I_E}{\beta+1}$$

$$I_E = \frac{V_{BB} - V_{BE}}{R_E + [R_{BB}/(\beta+1)]}$$

$$V_B = V_{BE} + I_E R_E$$



**Dr. D. M. Akbar Hussain**

**Department of Electronic Systems**

# Exercise 5.28

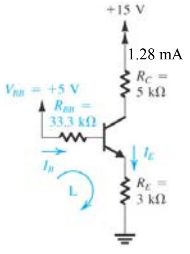
**5.28** If the transistor in the circuit of Fig. 5.40(a) is replaced with another having half the value of $\beta$ (i.e., $\beta = 50$), find the new value of $I_C$, and express the change in $I_C$ as a percentage.

**Ans.** $I_C = 1.15$ mA; $-10\%$

$$V_B - i_B R_B - V_{BE} - i_E R_E = 0$$

write $i_E$ in terms of $i_B$.

$$\% - Change = \frac{i_C - 1.28}{1.28} \times 100$$



(b)

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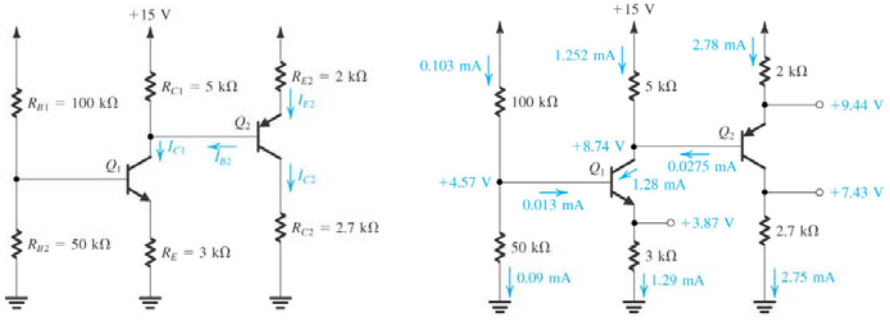
# Example 5.11

We wish to analyze the circuit in Fig. 5.41(a) to determine the voltages at all nodes and the currents through all branches.



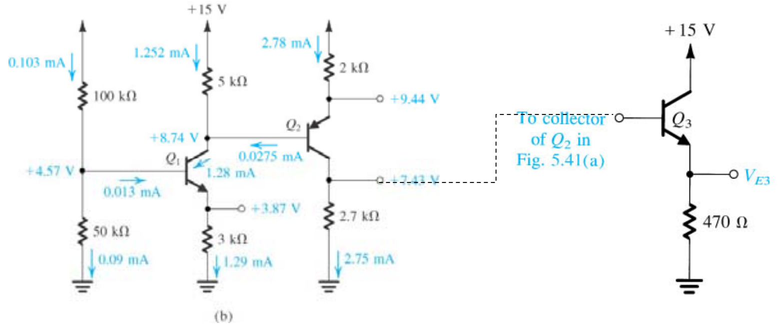
(a) (b)

# Exercises 5.29 & 5.30

**5.29** For the circuit in Fig. 5.41, find the total current drawn from the power supply. Hence find the power dissipated in the circuit.

**Ans.** 4.135 mA; 62 mW

**5.30** The circuit in Fig. E5.30 is to be connected to the circuit in Fig. 5.41(a) as indicated; specifically, the base of $Q_3$ is to be connected to the collector of $Q_2$. If $Q_3$ has $\beta = 100$, find the new value of $V_{C2}$ and the values of $V_{E3}$ and $I_{C3}$.



(b)

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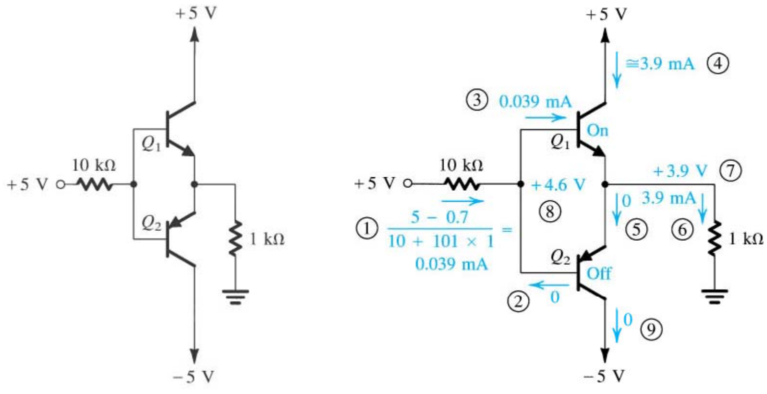
# Example 5.12

We desire to evaluate the voltages at all nodes and the currents through all branches in the circuit of Fig. 5.42(a). Assume $\beta = 100$.



(a) (b)

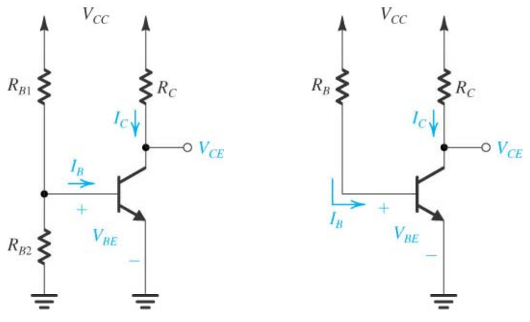
# Exercise 5.31

**5.31** Solve the problem in Example 5.12 with the voltage feeding the bases changed to +10 V. Assume that $\beta_{\text{min}} = 30$, and find $V_E$, $V_B$, $I_{C1}$, and $I_{C2}$.

**Ans.** +4.8 V; +5.5 V; 4.35 mA; 0

---

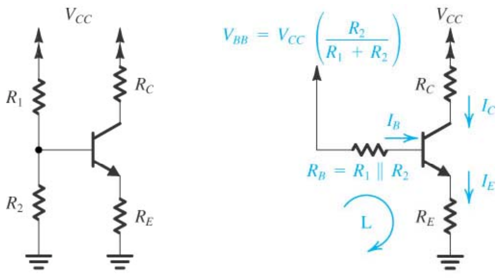
# Biasing BJT Amplifier Circuits



(a) (b)

Two obvious schemes for biasing the BJT: **(a)** by fixing $V_{BE}$; **(b)** by fixing $I_B$. Both result in wide variations in $I_C$ and hence in $V_{CE}$ and therefore are considered to be "bad." Neither scheme is recommended.

# Biasing BJT Amplifier Circuits



(a) (b)

$$I_B = \frac{I_E}{\beta + 1}$$

$$I_E = \frac{V_{BB} - V_{BE}}{R_E + [R_B/(\beta+1)]}$$

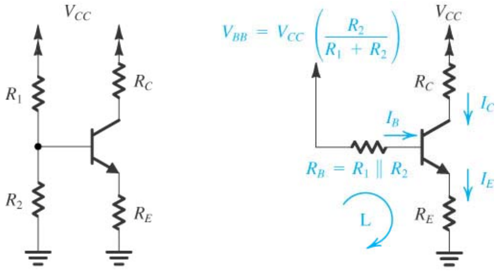
Classical biasing for BJTs using a single power supply: **(a)** circuit; **(b)** circuit with the voltage divider supplying the base replaced with its Thévenin equivalent. The small changes in the $V_{BE}$ are swept away by large value of $V_{BB}$. Also

$$R_E >> \frac{R_B}{\beta + 1}$$

---

# Example 5.13

We wish to design the bias network of the amplifier in Fig. 5.44 to establish a current $I_E = 1$ mA using a power supply $V_{CC} = +12$ V. The transistor is specified to have a nominal $\beta$ value of 100.

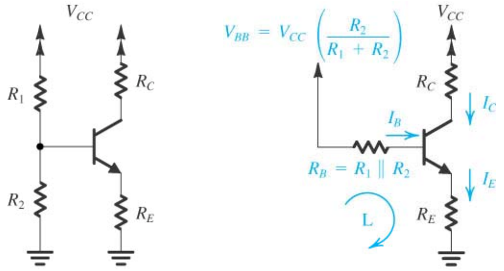


(a) (b)

# Exercise 5.32

**5.32** For design 1 in Example 5.13, calculate the expected range of $I_E$ if the transistor used has $\beta$ in the range of 50 to 150. Express the range of $I_E$ as a percentage of the nominal value ($I_E \simeq 1$ mA) obtained for $\beta = 100$. Repeat for design 2.

**Ans.** For design 1: 0.94 mA to 1.04 mA a 10% range; for design 2: 0.984 mA to 0.995 mA, a 1.1% range.



(a) (b)

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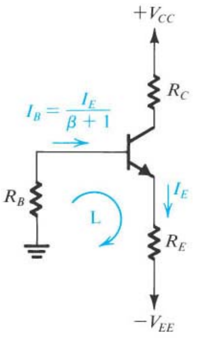
# Biasing BJT Amplifier Circuit with 2 PS

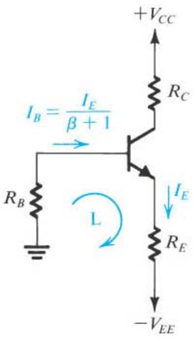


Biasing the BJT using two power supplies. Resistor $R_B$ is needed only if the signal is to be capacitively coupled to the base. Otherwise, the base can be connected directly to ground, or to a grounded signal source, resulting in almost total $\beta$-independence of the bias current.

# Exercise 5.33

**D5.33** The bias arrangement of Fig. 5.45 is to be used for a common-base amplifier. Design the circuit to establish a dc emitter current of 1 mA and provide the highest possible voltage gain while allowing for a maximum signal swing at the collector of ±2 V. Use +10-V and −5-V power supplies.

**Ans.** $R_B = 0$; $R_E = 4.3\ \text{k}\Omega$; $R_C = 8.4\ \text{k}\Omega$



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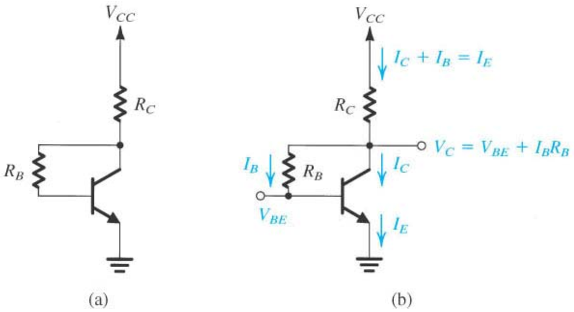
# Biasing BJT Amplifier Circuit with Feedback Resistor

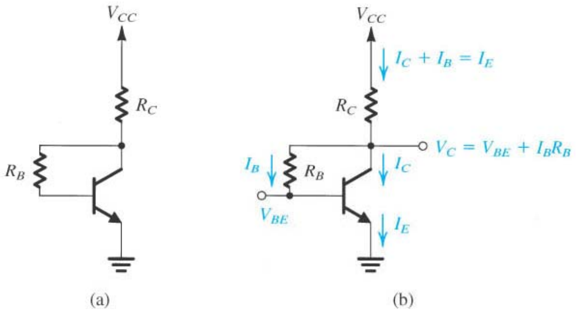


**(a)** A common-emitter transistor amplifier biased by a feedback resistor $R_B$. **(b)** Analysis of the circuit in (a).

# Exercise 5.34

**D5.34** Design the circuit of Fig. 5.46 to obtain a dc emitter current of 1 mA and to ensure a ±2-V signal swing at the collector; that is, design for $V_{CE} = +2.3$ V. Let $V_{CC} = 10$ V and $\beta = 100$.

**Ans.** $R_B = 162$ kΩ; $R_C = 7.7$ kΩ. Note that if standard 5% resistor values are used (Appendix G) we select $R_B = 160$ kΩ and $R_C = 7.5$ kΩ. This results in $I_E = 1.02$ mA and $V_C = +2.3$ V.



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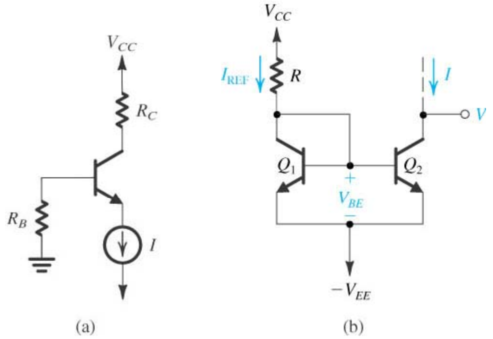
# Biasing using Constant Current Source

This has advantage that emitter current is independent of beta and base resistance, so base resistance can be made large to have high input resistance with out affecting the bias stability. It is more simplified design.
The circuit in (b) utilizes a matched transistors Q1 and Q2 (Q1 is connected as a diode), both transistors have high beta values, if we neglect both base current the current through Q1 is:

$$I_{REF} = \frac{V_{CC} - (-V_{EE}) - V_{BE}}{R}$$

As both transistors have same $V_{BE}$ so their collector current will be equal; $I = I_{REF}$.

By keeping V greater than $(-V_{EE} + V_{BE})$, we can guarantee that Q2 remains in active region and the current remains constant.



**(a)** A BJT biased using a constant-current source *I*. **(b)** Circuit for implementing the current source *I*.

# Exercise 5.35

5.35 For the circuit in Fig. 5.47(a) with $V_{CC} = 10$ V, $I = 1$ mA, $\beta = 100$, $R_B = 100$ kΩ, and $R_C = 7.5$ kΩ, find the dc voltage at the base, the emitter, and the collector. For $V_{EE} = 10$ V, find the required value of $R$ in order for the circuit of Fig. 5.47(b) to implement the current-source $I$.

Ans. −1 V; −1.7 V; +2.6 V; 19.3 kΩ

---

# Small Signal Operation

$$v_{BE} = V_{BE} + v_{be}$$

So we first set $v_{be}$ to zero, and following values of current and voltage are determined for DC.

$$I_C = I_S e^{v_{BE}/V_T}$$
$$I_E = I_C/\alpha$$
$$I_B = I_C/\beta$$
$$V_C = V_{CE} = V_{CC} - I_C R_C$$

<u>Collector Current & Transconductance</u>

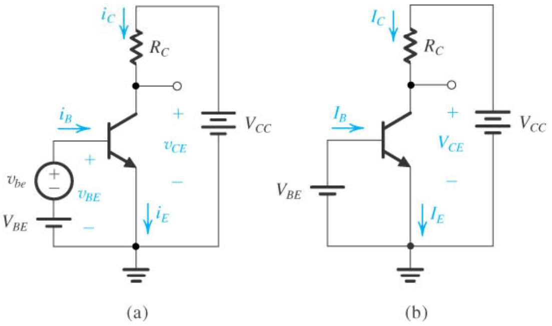
$$i_C = I_S e^{v_{BE}/V_T} = I_S e^{(V_{BE}+v_{be})/V_T}$$
$$i_C = I_S e^{V_{BE}/V_T} e^{v_{be}/V_T}$$
$$i_C = I_C e^{v_{be}/V_T}$$

if we suppose $v_{be} << V_T$

$$i_C = I_C\left(1 + \frac{v_{be}}{V_T}\right) \text{ this is only valid if } v_{be} \le 10mV$$

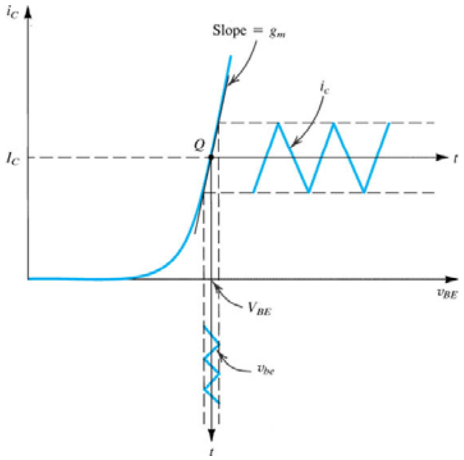
$$i_C = I_C + \frac{I_C v_{be}}{V_T} = I_C + i_c$$

$$i_c = \frac{I_C v_{be}}{V_T} = g_m v_{be}$$



**(a)** Conceptual circuit to illustrate the operation of the transistor as an amplifier. **(b)** The circuit of (a) with the signal source $v_{be}$ eliminated for dc (bias) analysis.

# Transconductance



Linear operation of the transistor under the small-signal condition: A small signal $v_{be}$ with a triangular waveform is superimposed on the dc voltage $V_{BE}$. It gives rise to a collector signal current $i_c$, also of triangular waveform, superimposed on the dc current $I_C$. Here, $i_c = g_m v_{be}$, where $g_m$ is the slope of the $i_C$–$v_{BE}$ curve at the bias point $Q$.

---

# Base, Emitter current and Gain

$$i_B = \frac{i_C}{\beta} = \frac{I_C + i_c}{\beta} = \frac{I_C}{\beta} + \frac{1}{\beta}\frac{I_C}{V_T} v_{be}$$

$$i_B = I_B + i_b$$

Small signal input resistance looking into base and emitter is;

$r_\pi \equiv \frac{v_{be}}{i_b}$ another alternative relationship $r_\pi = \frac{V_T}{I_B}$

$$i_E = \frac{i_C}{\alpha} = \frac{I_C + i_c}{\alpha} = \frac{I_C}{\alpha} + \frac{i_c}{\alpha} = I_E + i_e$$

Small signal resistance between base & emitter looking into emitter is;

$r_e \equiv \frac{v_{be}}{i_e}$ another alternative relationship $r_e = \frac{V_T}{I_E}$

We can find relationship between $r_\pi$ & $r_e$ as $r_\pi = (i_e / i_b) r_e$ & $r_\pi = (\beta + 1) r_e$

$$v_C = V_{CC} - i_C R_C = V_{CC} - (I_C + i_c) R_C = (V_{CC} - I_C R_C) - i_c R_C = V_C - i_c R_C$$

The small signal voltage

$$v_c = -i_c R_C = -g_m v_{be} R_C$$

$$A_v \equiv \frac{v_c}{v_{be}} = \frac{-g_m v_{be} R_C}{v_{be}} = -g_m R_C$$

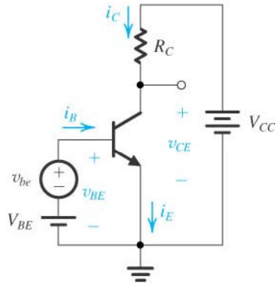
# Exercise 5.37 & 5.38

**5.37** A BJT having $\beta = 100$ is biased at a dc collector current of 1 mA. Find the value of $g_m$, $r_e$, and $r_\pi$ at the bias point.

**Ans.** 40 mA/V; 25 Ω; 2.5 kΩ

**5.38** In the circuit of Fig. 5.48(a), $V_{BE}$ is adjusted to yield a dc collector current of 1 mA. Let $V_{CC} = 15$ V, $R_C = 10$ kΩ, and $\beta = 100$. Find the voltage gain $v_c/v_{be}$. If $v_{be} = 0.005 \sin \omega t$ volts, find $v_C(t)$ and $i_B(t)$.

**Ans.** −400 V/V; $5 - 2 \sin \omega t$ volts; $10 + 2 \sin \omega t$ μA



(a)

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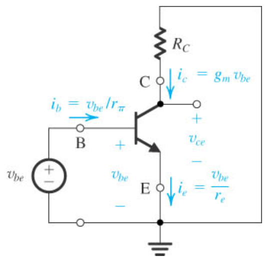
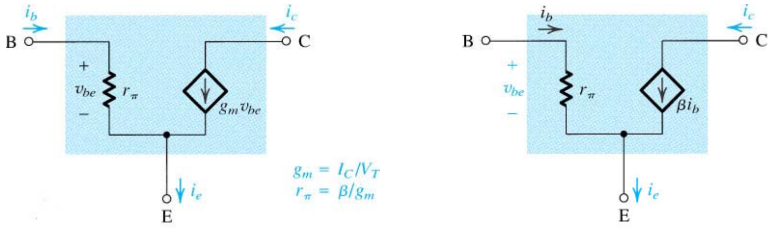
# Hybrid-π Model

The most widely used model.

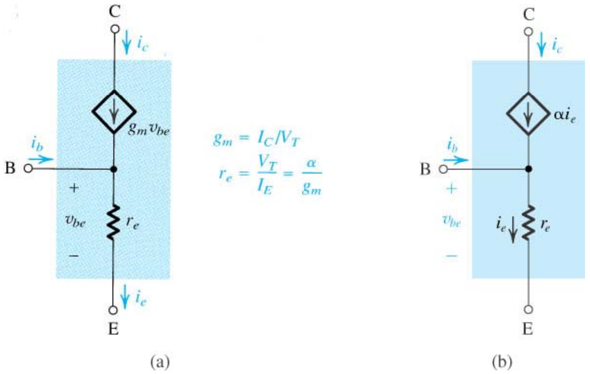




(a) (b)

Two slightly different versions of the simplified hybrid-$\pi$ model for the small-signal operation of the BJT. The equivalent circuit in **(a)** represents the BJT as a voltage-controlled current source (a transconductance amplifier), and that in **(b)** represents the BJT as a current-controlled current source (a current amplifier).

# The T Model



$$g_m = I_C / V_T$$
$$r_e = \frac{V_T}{I_E} = \frac{\alpha}{g_m}$$

Two slightly different versions of what is known as the *T model* of the BJT. The circuit in **(a)** is a voltage-controlled current source representation and that in **(b)** is a current-controlled current source representation. These models explicitly show the emitter resistance $r_e$ rather than the base resistance $r_\pi$ featured in the hybrid-$\pi$ model.

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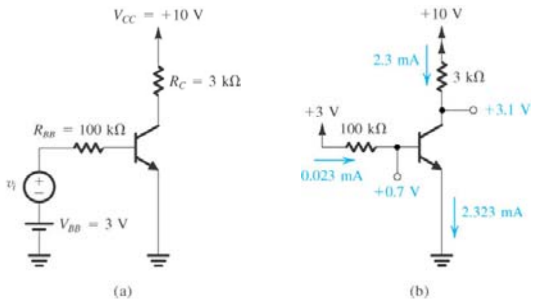
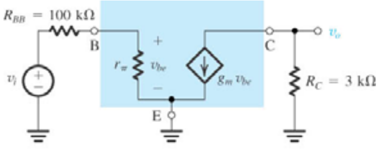
# Example 5.14

We wish to analyze the transistor amplifier shown in Fig. 5.53(a) to determine its voltage gain. Assume $\beta = 100$.

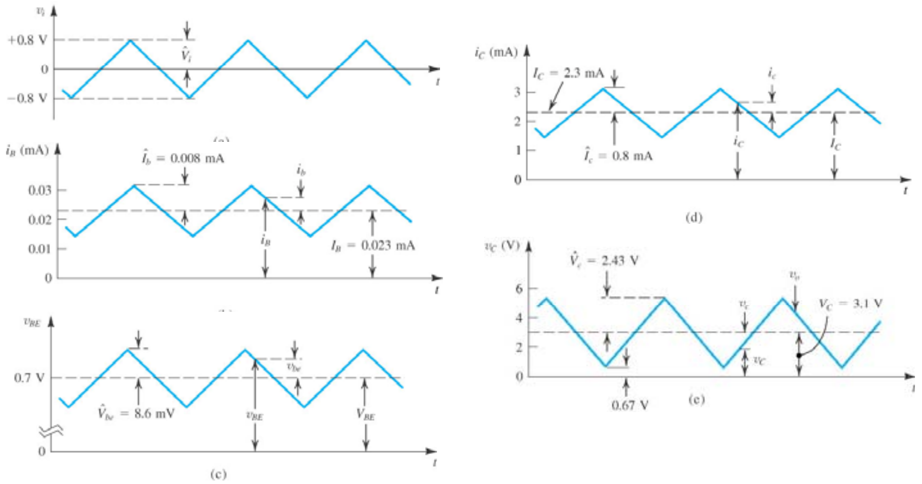




**(a)** circuit; **(b)** dc analysis; **(c)** small-signal model.

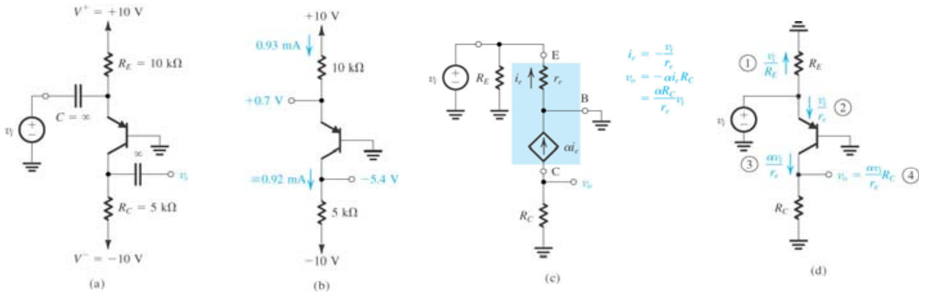
# Example 5.15

To gain more insight into the operation of transistor amplifiers, we wish to consider the waveforms at various points in the circuit analyzed in the previous example. For this purpose assume that $v_i$ has a triangular waveform. First determine the maximum amplitude that $v_i$ is allowed to have. Then, with the amplitude of $v_i$ set to this value, give the waveforms of $i_B(t)$, $v_{BE}(t)$, $i_C(t)$, and $v_C(t)$.



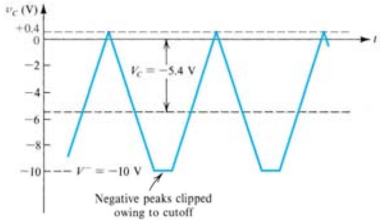
# Example 5.16

We need to analyze the circuit of Fig. 5.55(a) to determine the voltage gain and the signal waveforms at various points. The capacitor $C$ is a coupling capacitor whose purpose is to couple the signal $v_i$ to the emitter while blocking dc. In this way the dc bias established by $V^+$ and $V^-$ together with $R_E$ and $R_C$ will not be disturbed when the signal $v_i$ is connected. For the purpose of this example, $C$ will be assumed to be very large and ideally infinite—that is, acting as a perfect short circuit at signal frequencies of interest. Similarly, another very large capacitor is used to couple the output signal $v_o$ to other parts of the system.

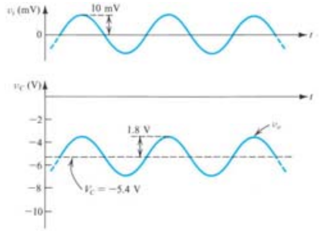


**(a)** circuit; **(b)** dc analysis; **(c)** small-signal model; **(d)** small-signal analysis performed directly on the circuit.

# Example 5.16



Distortion in output signal due to transistor cutoff. Note that it is assumed that no distortion due to the transistor nonlinear characteristics is occurring.

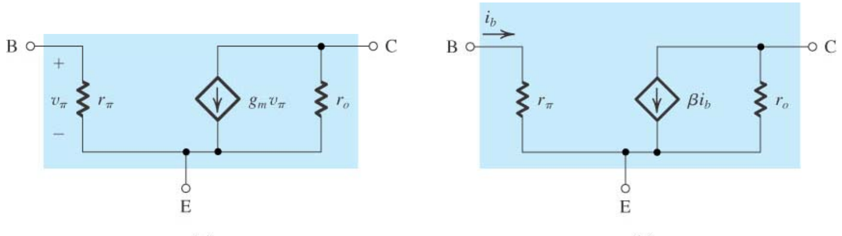


Input and output waveforms for the circuit of Fig. 5.55. Observe that this amplifier is non-inverting, a property of the common-base configuration.

---

# Small Signal Model to Account for Early Effect

We have seen that the collector current not only depend on $v_{BE}$ but also on $v_{CE}$, so the dependence on $v_{CE}$ can be modelled by assigning a finite output resistance to the controlled current source in the hybrid pi model.



$$r_o = \frac{(V_A + V_{CE})}{I_C} \approx \frac{V_A}{I_C}$$

$$v_o = -g_m v_{be} (R_C \,||\, r_o)$$

The hybrid-$\pi$ small-signal model, in its two versions, with the resistance $r_o$ included.

# Exercise 5.40

**5.40** The transistor in Fig. E5.40 is biased with a constant current source $I = 1$ mA and has $\beta = 100$ and $V_A = 100$ V. (a) Find the dc voltages at the base, emitter, and collector. (b) Find $g_m$, $r_\pi$, and $r_o$. (c) If terminal Z is connected to ground, X to a signal source $v_{sig}$ with a source resistance $R_{sig} = 2$ kΩ, and Y to an 8-kΩ load resistance, use the hybrid-$\pi$ model of Fig. 5.58(a), to draw the small-signal equivalent circuit of the amplifier. (Note that the current source $I$ should be replaced with an open circuit.) Calculate the overall voltage gain $v_y/v_{sig}$. If $r_o$ is neglected what is the error in estimating the gain magnitude? (*Note:* An infinite capacitance is used to indicate that the capacitance is sufficiently large that it acts as a short circuit at all signal frequencies of interest. However, the capacitor still blocks dc.)

**Ans.** (a) −0.1 V, −0.8 V, +2 V; (b) 40 mA/V, 2.5 kΩ, 100 kΩ; (c) −77 V/V, +3.9%