CHAPTER 14

Output Stage and Power Amplifiers

Lecture # 9

What is Expected from Output Stage ?

Most important function of the output stage of an amplifier is to provide low output resistance so that it can deliver the output signal to the load without any gain loss.

Output is the last stage so it deals normally with large signal model so the small signal models usually do not applicable or cannot be used in a straight manner.

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THD

Goodness of the output stage design is measured as "Total Harmonic Distortion (THD)" which the final stage produce and it is rms value of the output signal excluding the fundamental component (expressed as a %age of the rms of the fundamental).

Challenge

The challenge here is to deliver the required power to the load in an efficient manner.

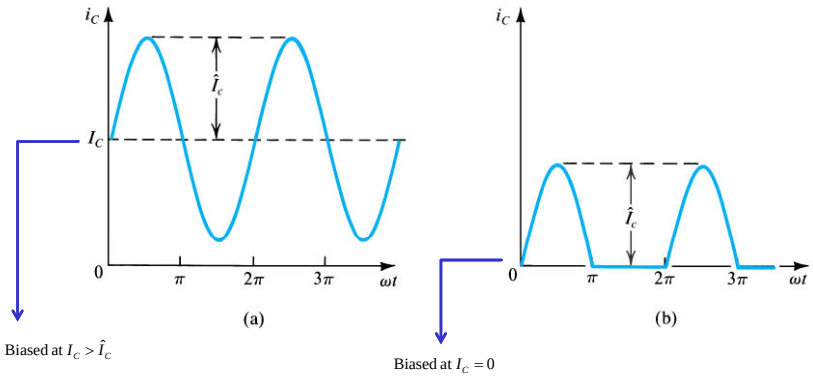
Which essentially meaning that the power dissipation should be as low as possible (the junction temperature remains under control which can result in damaging the transistor).

High Power

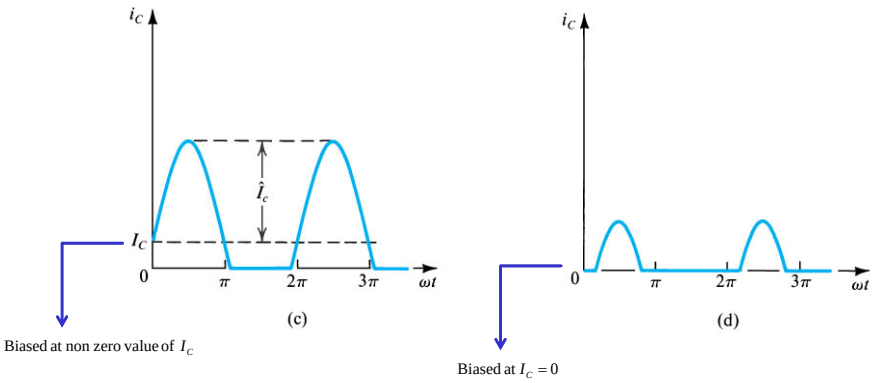
When we say "High Power" it generally means 1 W.

Classification

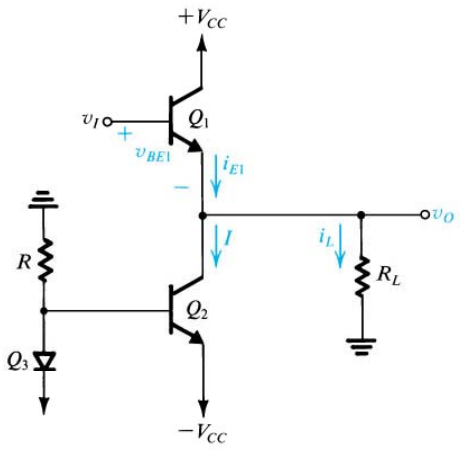
It is based on the collector current waveform when a signal is applied at the input.



Classification



Class A Output Stage

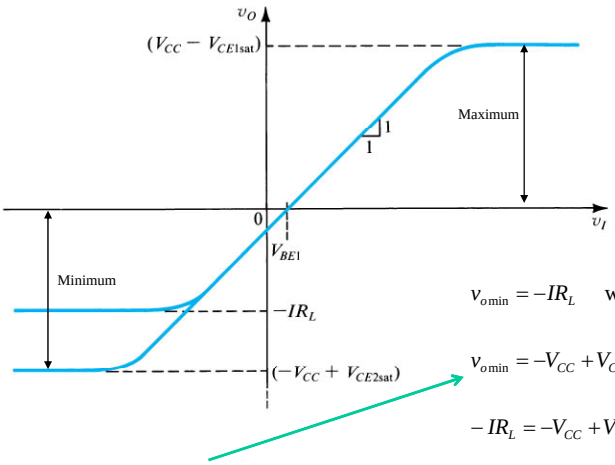


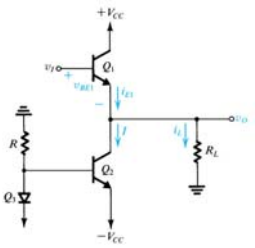
$$i_{E1} = I + i_L$$

$$v_o = v_I - v_{BE1}$$

$$v_{o\max} = V_{CC} - V_{CE1sat}$$

Transfer Characteristics





$v_{o\min} = -IR_L$ when Q_1 is off

$v_{o\min} = -V_{CC} + V_{CE2sat}$ when Q_2 in saturation

$-IR_L = -V_{CC} + V_{CE2sat}$

$$I \geq \frac{|-V_{CC} + V_{CE2sat}|}{R_L}$$

The absolute lowest output voltage can only be achieved provided the bias current I is greater than the magnitude of the corresponding load current.

Exercise 14.1 & 14.2

D14.1 For the emitter follower in Fig. 14.2, $V_{CC} = 15$ V, $V_{CEsat} = 0.2$ V, $V_{BE} = 0.7$ V and constant, and β is very high. Find the value of R that will establish a bias current sufficiently large to allow the largest possible output signal swing for $R_L = 1$ kΩ. Determine the resulting output signal swing and the minimum and maximum emitter currents.

Ans. 0.97 kΩ; −14.8 V to +14.8 V; 0 to 29.6 mA

14.2 For the emitter follower of Exercise 14.1, in which $I = 14.8$ mA, consider the case in which v_O is limited to the range −10 V to +10 V. Let Q_1 have $v_{BE} = 0.6$ V at $i_C = 1$ mA, and assume $\alpha \simeq 1$. Find v_I corresponding to $v_O = -10$ V, 0 V, and +10 V. At each of these points, use small-signal analysis to determine the voltage gain v_o/v_i. Note that the incremental voltage gain gives the slope of the v_O-versus-v_I characteristic.

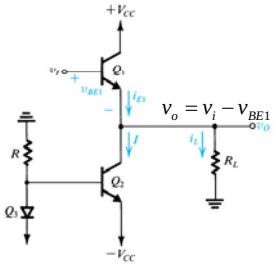
Ans. −9.36 V, 0.67 V, 10.68 V; 0.995 V/V, 0.998 V/V, 0.999 V/V

$i_L =$

$i_{E1} = I + i_L$

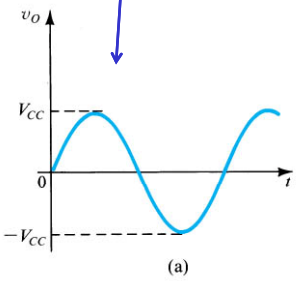
$$v_{BE1} = v_{BE} + V_T \ln\left(\frac{i_{E1}}{i_C}\right)$$

$$r_{e1} = \frac{V_T}{i_{E1}}$$

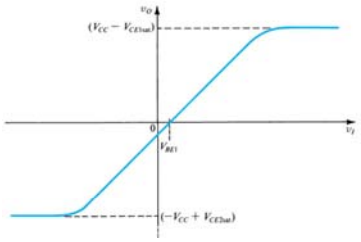


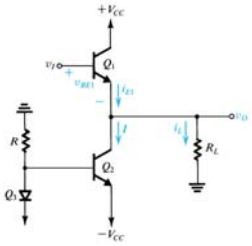
Signal Wave Forms

Maximum signal waveform in the class A output stage, when biased at current I (it will swing from $+V_{CC}$ to $-V_{CC}$, neglecting v_{CEsat} .



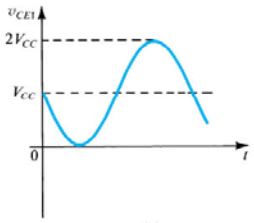
(a)



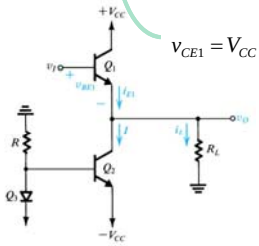


Signal Wave Forms

When Q_1 is in saturation the output voltage is approximately, V_{CC} (when no signal is applied).

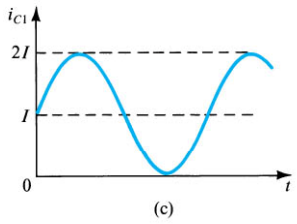


(b)

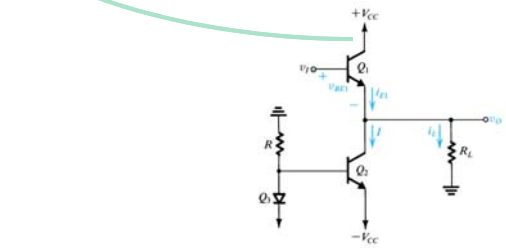


$$v_{CE1} = V_{CC} - v_o$$

Signal Wave Forms

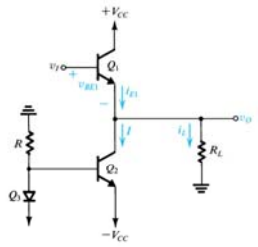


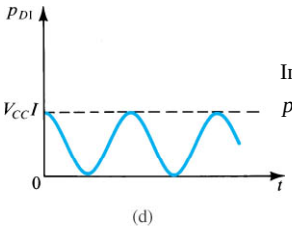
(c)



As amplifier is biased at I so the current in collector of Q1 will have this shape.

Power Dissipation





(d)

Instantaneous power dissipation

$$p_{D1} = v_{CE1} i_{C1}$$

Class A has maximum instantaneous power dissipation when there is no input signal and if that happens for long period of time the transistor Q_1 must withstand a continuous power dissipation of V_{CC} x I.

The P_D in Q_1 depend upon R_L: Maximum ($R_L = \infty$) or Minimum (Short Circuit $R_L = 0$).
If R_L is infinity, meaning collector current in Q_1 is equal to I, which is a constant so power dissipation will depend on the value of output v_o. Maximum P_D will occur when $v_o = -V_{CC}$ we know $v_{CE1} = V_{CC} - v_o$ and if we put $v_o = -V_{CC}$, $v_{CE1} = 2V_{CC}$ so $p_{D1} = 2V_{CC}$ x I.

If R_L = 0, meaning short circuit, theoretically, with positive voltage infinite current will occur so it can damage the transistor.

Power Conversion Efficiency

$$\eta = \frac{Load - power\ (P_L)}{Supply - power\ (P_S)}$$

$$P = VI = I^2 R$$

$$P_L = \frac{\left(\hat{V}_o/\sqrt{2}\right)^2}{R_L} = \frac{1}{2}\frac{\hat{V}_o^{\,2}}{R_L}$$

$$P_S = 2V_{CC} I$$

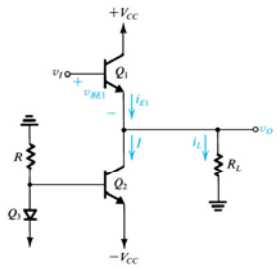
$\eta = \frac{1}{4}$ Maximum efficiency can be obtained only when $\hat{V}_o = V_{CC} = IR_L$

Since $\hat{V}_o \le V_{CC}$ and $\hat{V}_o \le IR_L$

Exercise 14.3

14.3 Consider the emitter follower in Fig. 14.2 with V_{CC} = 10 V, I = 100 mA, and R_L = 100 Ω. Find the power dissipated in Q_1 and Q_2 under quiescent conditions (v_O = 0). For a sinusoidal output voltage of maximum possible amplitude (neglecting V_{CEsat}), find the average power dissipation in Q_1 and Q_2. Also find the load power.

Ans. 1 W, 1 W; 0.5 W, 1 W; 0.5 W

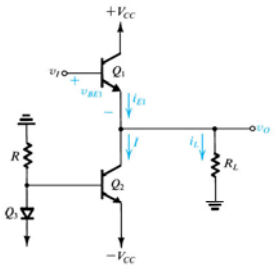


Exercise 14.4

14.4 For the emitter follower of Fig. 14.2, let $V_{CC} = 10$ V, $I = 100$ mA, and $R_L = 100\ \Omega$. If the output voltage is an 8-V-peak sinusoid, find the following: (a) the power delivered to the load; (b) the average power drawn from the supplies; (c) the power-conversion efficiency.

Ignore the loss in Q_3 and R.

Ans. 0.32 W; 2 W; 16%



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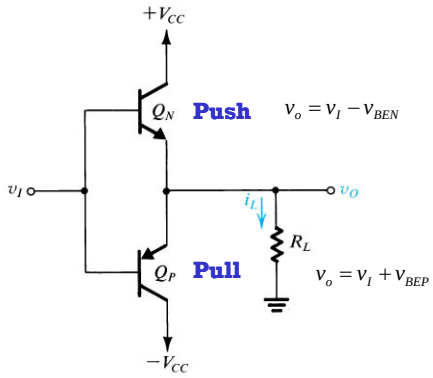
Class B Output Stage



It is biased at zero current and any of the above transistors will conducts once a signal is present at the input.

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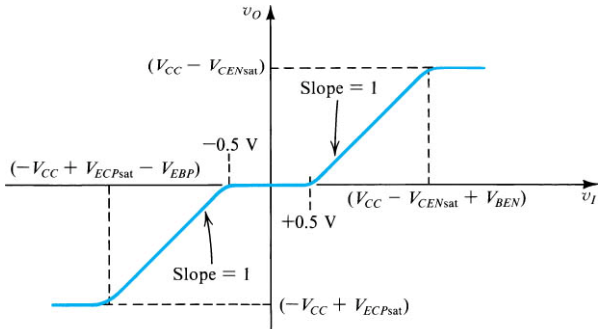
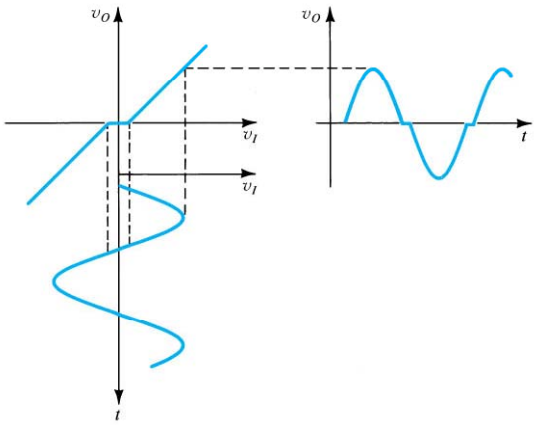
Transfer Characteristics of Class B



Crossover Distortion



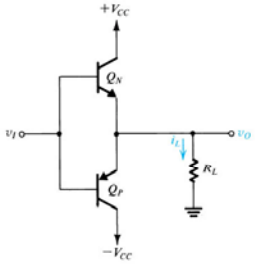
Power Conversion Efficiency in Class B

$$P_L = \frac{1}{2}\frac{\hat{V}_o^2}{R_L}$$

The current drawn from each supply consists of half-sine waves of peak amplitude; $\frac{\hat{V}_o}{R_L}$

Therefore, average current from both supplies = $\frac{\hat{V}_o}{\pi R_L}$

So the total supply power = 2 V I = $P_S = 2V_{CC}\frac{\hat{V}_o}{\pi R_L}$



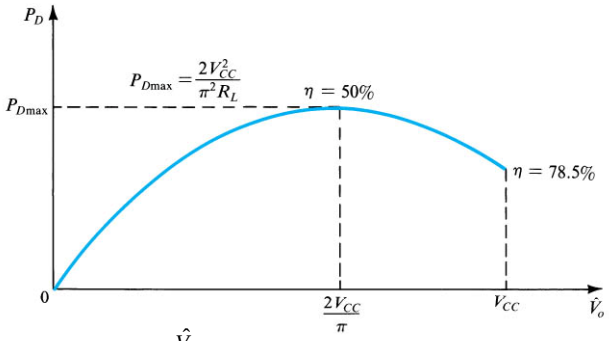
$$\eta = \frac{P_L}{P_S} = \frac{\left(\frac{1}{2}\frac{\hat{V}_o^2}{R_L}\right)}{\left(\frac{2}{\pi}\frac{\hat{V}_o}{R_L}V_{CC}\right)} = \frac{\pi}{4}\frac{\hat{V}_o}{V_{CC}}$$

$\eta = \frac{\pi}{4}$ so maximum efficiency when V_o is maximum(V_{CC})

It comes out to be 78.5 %.

Power Dissipation of Class B

It is unlike class A where the maximum power dissipation occurs under quiescent conditions, in class B it is zero at quiescent conditions.
Also, as the transistors conducts alternatively so each one dissipate half the power.

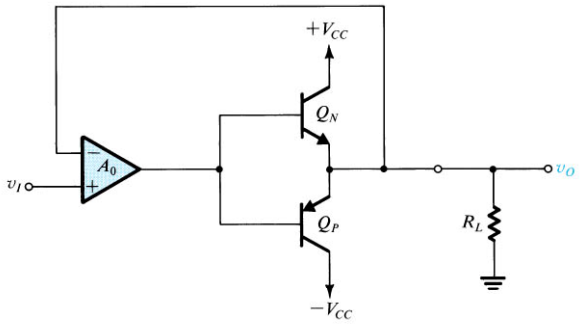


$$P_S = 2V_{CC}\frac{\hat{V}_o}{\pi R_L}$$

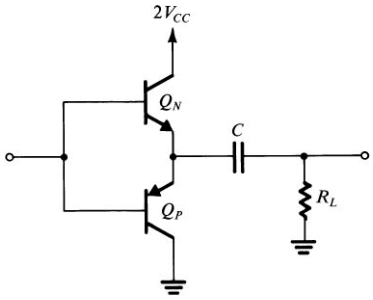
$$P_L = \frac{1}{2}\frac{\hat{V}_o^2}{R_L}$$

$$P_D = P_S - P_L$$

Crossover Distortion Removal



Single Supply Circuit for Class B



Exercise 14.5

14.5 For the class B output stage of Fig. 14.5, let $V_{CC} = 6$ V and $R_L = 4\ \Omega$. If the output is a sinusoid with 4.5-V peak amplitude, find (a) the output power; (b) the average power drawn from each supply; (c) the power efficiency obtained at this output voltage; (d) the peak currents supplied by v_I, assuming that $\beta_N = \beta_P = 50$; (e) the maximum power that each transistor must be capable of dissipating safely.

Ans. (a) 2.53 W; (b) 2.15 W; (c) 59%; (d) 22.1 mA; (e) 0.91 W

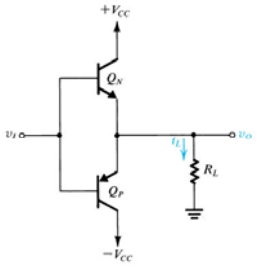
P_L

$P_+ \quad P_-$

η

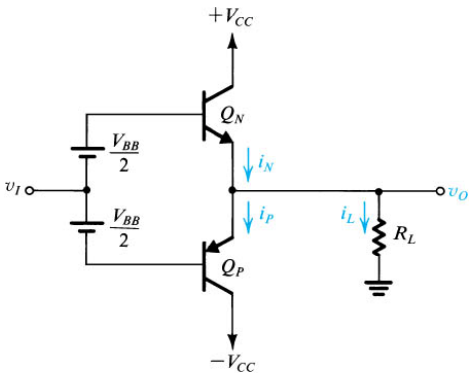
I_B Peak current supplied by v_I

$P_{D\max}$



Class AB

Class AB output stage. A bias voltage V_{BB} is applied between the bases of Q_N and Q_P, giving rise to a bias current I_Q . Thus, for small v_I, both transistors conduct and crossover distortion is almost completely eliminated.



$$i_N = i_P = I_Q = I_S e^{v_{BB}/2V_T}$$

$$v_o = v_I + \frac{V_{BB}}{2} - v_{BEN}$$

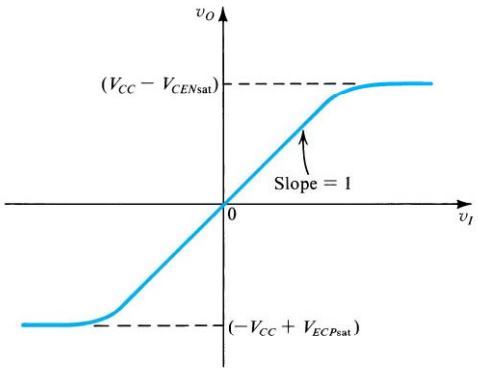
$$i_N = i_P + i_L$$

$$v_{BEN} + v_{BEP} = V_{BB}$$

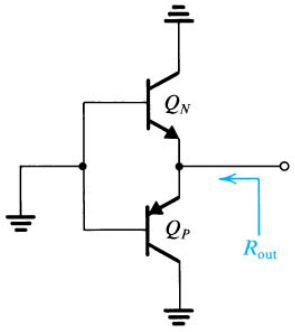
$$V_T \ln\frac{i_N}{I_S} + V_T \ln\frac{i_P}{I_S} = 2V_T \ln\frac{I_Q}{I_S}$$

$$i_N i_P = I_Q^2$$

Class AB Characteristics



Output Resistance of Class AB



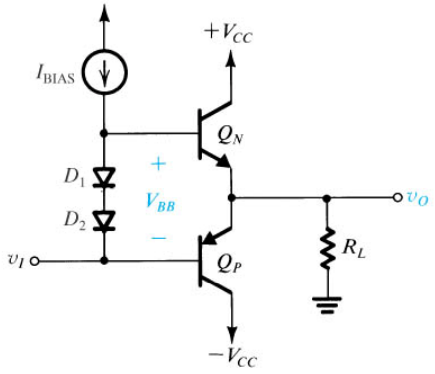
$$R_{out} = r_{eN} \parallel r_{eP}$$

$$r_{eN} = \frac{V_T}{i_N}$$

$$R_{out} = \frac{V_T}{i_N + i_P}$$

Biasing Class AB

A class AB output stage utilizing diodes for biasing. If the junction area of the output devices, Q_N and Q_P, is n times that of the biasing devices D_1 and D_2, and a quiescent current $I_Q = nI_{BIAS}$ flows in the output devices.



Class AB operates in the same way as Class B, the power dissipation is almost identical to Class B. The only difference is that under quiescent conditions the Class AB dissipates V_{CC} I_Q per transistor.

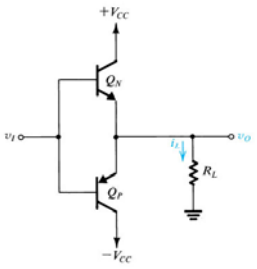
Exercise 14.7 & 14.8

14.7 For the circuit of Example 14.2, find i_N and i_P for $v_O = +10$ V and $v_O = -10$ V.

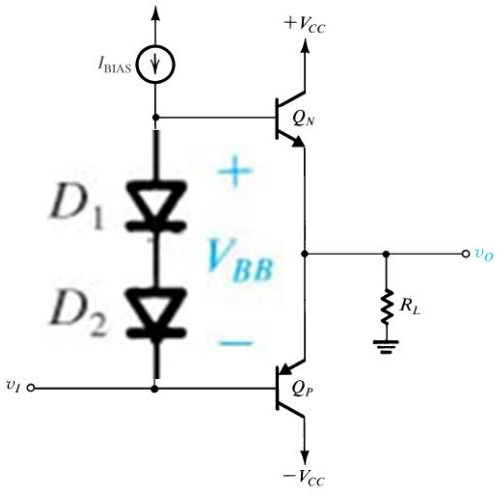
Ans. 100.1 mA, 0.1 mA; 0.8 mA, 100.8 mA

14.8 If the collector current of a transistor is held constant, its v_{BE} decreases by 2 mV for every 1°C rise in temperature. Alternatively, if v_{BE} is held constant, then i_C increases by approximately $g_m \times 2$ mV for every 1°C rise in temperature. For a device operating at $I_C = 10$ mA, find the change in collector current resulting from an increase in temperature of 5°C.

Ans. 4 mA



Biasing Class AB with V_{BE} Multiplier



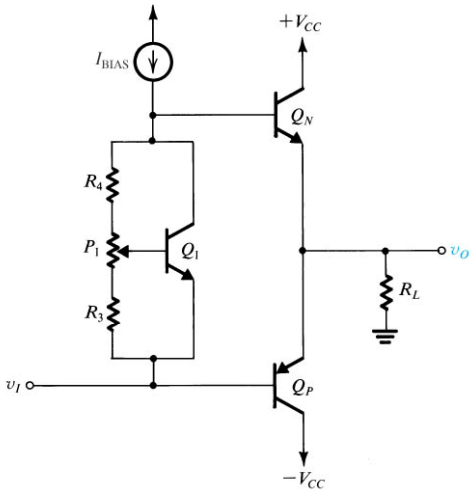
$$I_R = \frac{V_{BE1}}{R_1}$$

$$V_{BB} = I_R(R_1 + R_2)$$

$$V_{BB} = V_{BE1}\left(1 + \frac{R_2}{R_1}\right)$$

Biasing Class AB with V_{BE} Multiplier

A discrete-circuit class AB output stage with a potentiometer used in the V_{BE} multiplier. The potentiometer is adjusted to yield the desired value of quiescent current in Q_N and Q_P.



Exercise 14.9

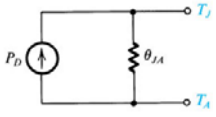
14.9 Consider a V_{RF} multiplier with $R_1 = R_2 = 1.2$ kΩ, utilizing a transistor that has $V_{BE} = 0.6$ V at $I_C = 1$ mA, and a very high β. (a) Find the value of the current I that should be supplied to the multiplier to obtain a terminal voltage of 1.2 V. (b) Find the value of I that will result in the terminal voltage changing (from the 1.2-V value) by +50 mV, +100 mV, +200 mV, –50 mV, –100 mV, –200 mV.

Ans. (a) 1.5 mA; (b) 3.24 mA, 7.93 mA, 55.18 mA, 0.85 mA, 0.59 mA, 0.43 mA

Properties of Power BJTs

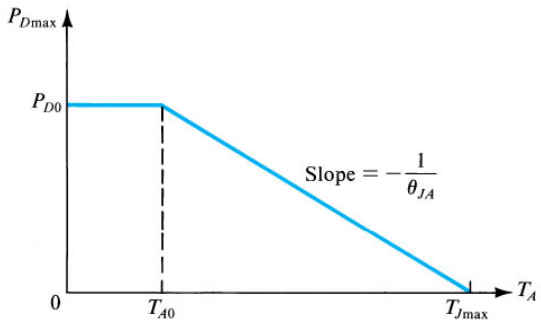
- Power BJTs differ in size, shape due to the ampere range, power dissipation etc.
- Large amount of power is dissipated in the collector-base junction in power BJTs. So the junction temperature increases which should not go beyond some maximum limit T_{Jmax} otherwise it will damage the junction permanently (For silicon the range of T_{Jmax} is 150 – 200 degrees C.
- Suppose a transistor is operating in free air with no special cooling mechanism, heat generated will be conducted away from junction to the casing of the transistor and from there to air and it can be expressed as:
- $T_J - T_A = P_D \theta_{JA}$.

  T_J is junction temperature, T_A is ambience temperature, P_D is power dissipation and θ_{JA} is the thermal resistance between junction and ambience.
- To keep T_{Jmax} minimum, θ_{JA} should be as small as possible. (In other words we wish to draw large amount of current but would like not to raise the junction temperature above T_{Jmax}.
- We can represent this thermal-conduction process as an electrical equivalent circuit.



P_D Vs Temperature

Maximum allowable power dissipation versus ambient temperature for a BJT operated in free air. This is known as a "power-de-rating" curve.

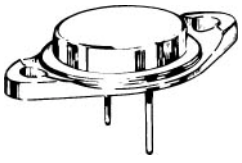


$$\theta_{JA} = \frac{T_{J\max} - T_{A0}}{P_{D0}}$$

$$P_{D\max} = \frac{T_{J\max} - T_A}{\theta_{JA}}$$

Heat Sink & Transistor Case

The popular TO3 package for power transistors. The case is metal with a diameter of about 2.2 cm; the outside dimension of the "seating plane" is about 4 cm. The seating plane has two holes for screws to bolt it to a heat sink. The collector is electrically connected to the case. Therefore an electrically insulating but thermally conducting spacer is used between the transistor case and the "heat sink."



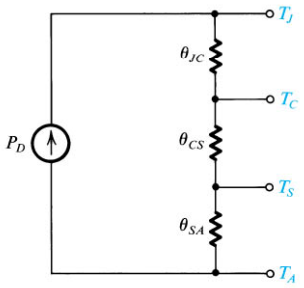
$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

Heat Sink & Transistor Case

Electrical analog of the thermal conduction process when a heat sink is utilized.

$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

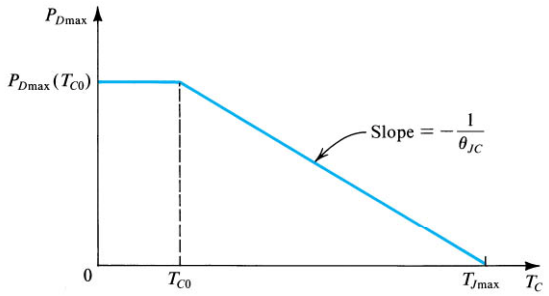
$$T_J - T_A = P_D(\theta_{JC} + \theta_{CS} + \theta_{SA})$$



Heat Sink & Transistor Case

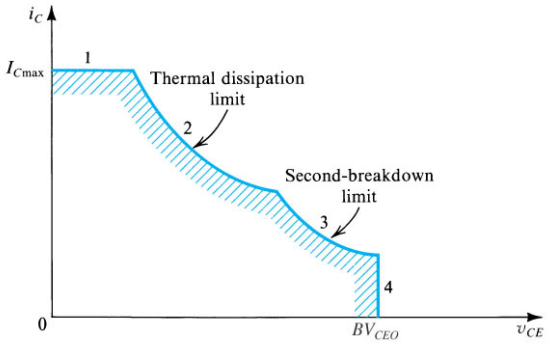
The manufacturer also supplies de-rating curve for power dissipation and the case temperature as shown below and the maximum power dissipation is given as:

$$P_{D\max} = \frac{T_{J\max} - T_C}{\theta_{JC}}$$



Maximum allowable power dissipation versus transistor-case temperature.

Safe Operating Area for BJTs



Exercise 14.11

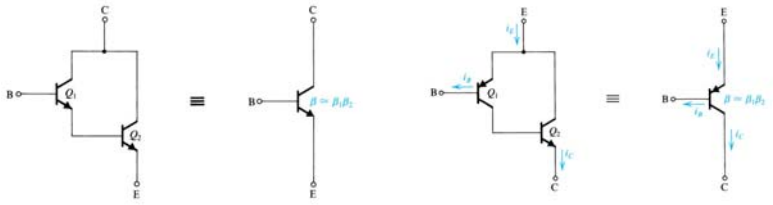
14.10 The 2N6306 power transistor is specified to have $T_{Jmax} = 200°C$ and $P_{Dmax} = 125$ W for $T_C \leq 25°C$. For $T_C \geq 25°C$, $\theta_{JC} = 1.4°C/W$. If in a particular application this device is to dissipate 50 W and operate at an ambient temperature of 25°C, find the maximum thermal resistance of the heat sink that must be used (i.e., θ_{SA}). Assume $\theta_{CS} = 0.6°C/W$. What is the case temperature, T_C?

Ans. 1.5°C/W; 130°C

14.11 (*Note:* Although very instructive, this exercise is rather long.) Consider the circuit of Fig. 14.24 with $R_1 = R_2 = 5$ kΩ, $R_3 = R_4 = 0$ Ω, and $V_{CC} = 15$ V. Let the transistors be matched with $I_S = 3.3 \times 10^{-14}$ A, $n = 1$, and $\beta = 200$. (These are the values used in the LH002 manufactured by National Semiconductor, except that $R_3 = R_4 = 2$ Ω there.) (a) For $v_I = 0$ and $R_L = \infty$, find the quiescent current in each of the four transistors and v_O. (b) For $R_L = \infty$, find i_{C1}, i_{C2}, i_{C3}, i_{C4}, and v_O for $v_I = +10$ V and -10 V. (c) Repeat (b) for $R_L = 100$ Ω.

Ans. (a) 2.87 mA; 0 V; (b) for $v_I = +10$ V: 0.88 mA, 4.87 mA, 1.95 mA, 1.95 mA, +9.98 V; for $v_I = -10$ V: 4.87 mA, 0.88 mA, 1.95 mA, 1.95 mA, –9.98 V; (c) for $v_I = +10$ V: 0.38 mA, 4.87 mA, 100 mA, 0.02 mA, +9.86 V; for $v_I = -10$ V: 4.87 mA, 0.38 mA, 0.02 mA, 100 mA, –9.86 V

Use of Compound Devices



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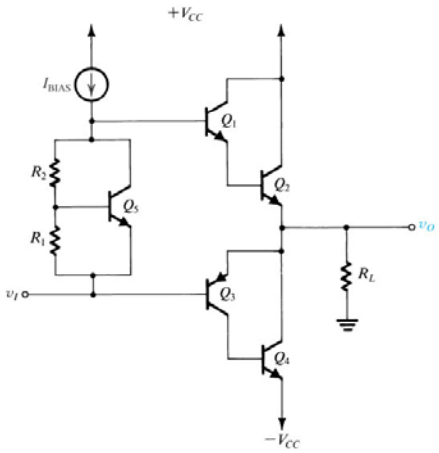
Class AB Output Stage with Darlington Pair



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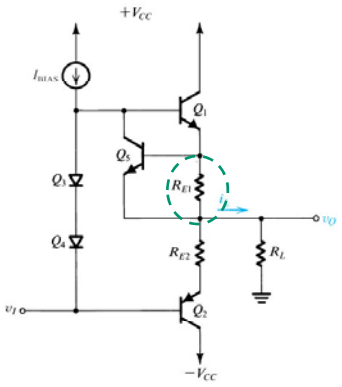
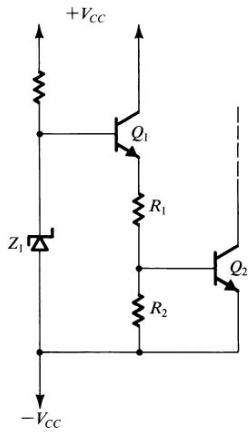
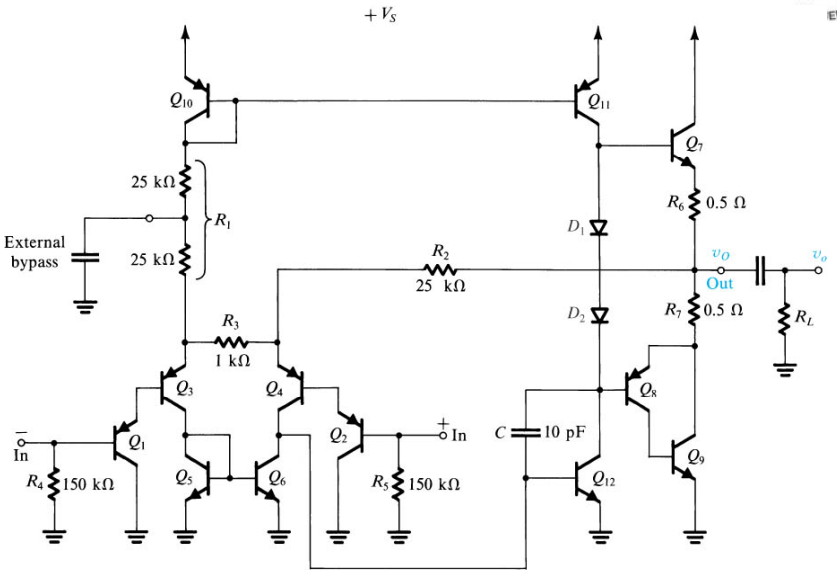
Short Circuit Protection



Thermal Shutdown



Example LM380 IC Power Amplifier



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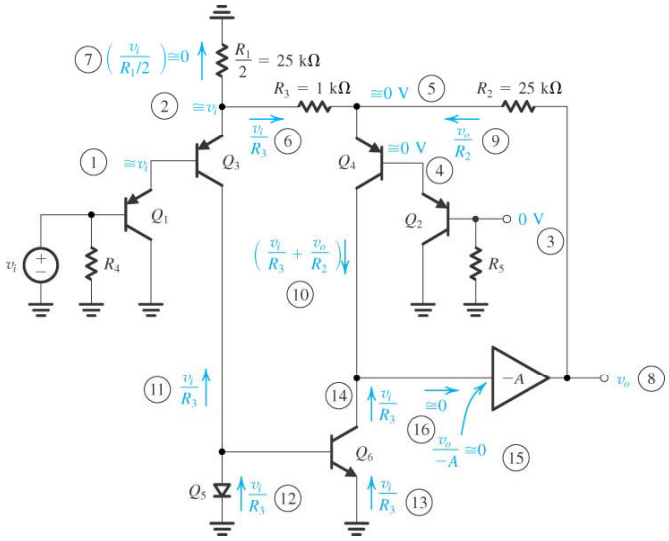
Analysis of LM380



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