

Digital Control Lecture 3



- 1 Digital Controller Design
- 2 Lead Compensator for Antenna Design Example



What have we talked about in MM2?

- Sampling rate selection
- Equivalents between continuous & digital Systems

Sampling theorem

Theoretical lower limit



 ω_s : sampling frequency ω_b : required closed-loop bandwidth

Smooth response

Practical limits

$$20 < rac{\omega_s}{\omega_b} < 40$$

 ω_s : sampling frequency ω_b : required closed-loop bandwidth

Sampling Rate Selection Equivalents Between Continuous and Digital Systems Exercises

Sampling Theorem Smoothness Effect of Noise

Requirements to prefilter

Breakpoint of prefilter, ω_c

$$\omega_b < \omega_c < \frac{\omega_s}{2}$$

- ω_s : sampling frequency
- ω_b : required closed-loop bandwidth
- ω_c: breakpoint of filter

Prefilter should filter lowest noise frequencies while not disturbing highest system frequencies!



Sampling Rate Selection Equivalents Between Continuous and Digital Systems Exercises

Sampling Effect System Specifications

Accommodating for sampling effect delay

Approximation of delay

$$e^{-sT/2} pprox rac{2/T}{s+2/T}$$

Accommodation

Investigate effect of half-sample delay on continuous system before digitizing:

- Root locus wrt. T
- Analyze using frequency based methods
 - Effect on phase margin/damping



Sampling Rate Selection Equivalents Between Continuous and Digital Systems Exercises

Sampling Effect System Specifications

Digital equivalents of continuous-time specifications

Transient response

- Overshoot/damping, M_p, ζ
- Rise time, ω_n
- Settling time, ω_n, ζ, σ

Steady-state response

- Steady-state: $z \to 1$, $(\lim_{k\to\infty} f(k) = \lim_{z\to 1} (z-1)F(z))$
- System type: number of pure integrators in open-loop,
 (z = 1)
- System input

• Parabola,
$$\frac{T^2}{2} \frac{z(z+1)}{(z-1)^3}$$

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Outline



- 2 Lead Compensator for Antenna Design Example
 - Effect of Sample Times
 - Accommodation for Sampling Delay
 - Effect of Sampling Method



Emulation Method for Digital Control

Digital Controller Design

Digital controller can be obtained using:

- Emulation, which finds the discrete equivalent of a continuous controller
- Direct discrete design (next lecture)



Frequency Issues

Continuous Systems

For a minimum-phase transfer function, the phase is uniquely determined by the magnitude curve:

 $\angle G(j\omega) \approx n \times 90^{\circ}$

where *n* is the slope of $G(j\omega)$ in units of decade of amplitude

Discrete Systems

The amplitude and phase relationship is lost! The prediction of stability from the amplitude curve alone for minimum-phase systems is lost It is typically necessary to determine both magnitude and phase for discrete systems



Emulation Method

- A continuous controller is designed
- 2 Sample time is selected
- Oiscrete equivalent is computed
- Evaluation of design



| Digital Controller Design | Effect of Sample Times |
|---|----------------------------------|
| Lead Compensator for Antenna - Design Example | Accommodation for Sampling Delay |
| Exercises | Effect of Sampling Method |

Outline

Digital Controller DesignEmulation Method for Digital Control

2 Lead Compensator for Antenna - Design Example

- Effect of Sample Times
- Accommodation for Sampling Delay
- Effect of Sampling Method



Case Study: Antenna Control

General System Model:

$$J\ddot{\theta} + B\dot{\theta} = T_c + T_d$$

Discarding the disturbances T_d gives the transfer function:

$$rac{\Theta(s)}{U(s)}=rac{1}{s\left(rac{s}{a}+1
ight)}$$
 where $a=rac{B}{I}=0.1$ and $u(t)=rac{T_c(t)}{B}.$

Design Specifications:

- \bullet Overshoot to a step input less than 16% (PM $\approx 55)$
- Settling time to 1% in less than 10s
- Tracking error to ramp of slope $0.01\frac{rad}{sec}$ less than 0.01rad
- Sampling time to give at least 10 samples in a rise-time



Digital Controller Design Lead Compensator for Antenna - Design Example Exercises Effect of Sampler Times Accommodation for Sampling Delay Effect of Sampling Method

Lead Compensator Design for Antenna (FC pp. 375)

Step 1

Design the low frequency gain K with respect to the steady-state error specification

Antenna system case: K = 1

Step 2

Determine the needed phase lead

```
sys=tf(1,[10 1 0]);
margin(sys)
```

PM=18 at $\omega = 0.308$



Digital Controller Design Lead Compensator for Antenna - Design Example Exercises Effect of Sample Times Accommodation for Sampling Delay Effect of Sampling Method

Lead Compensator Design for Antenna (FC pp. 375)

Step 3

Using lead contribution of $\phi_{max}=$ 45 should result in PM=63 which is 8 more than needed.

Step 4

Determine:

$$\alpha = \frac{1 - \sin \phi_{max}}{1 + \sin \phi_{max}} = \frac{1 - \sin 45}{1 + \sin 45} = 0.1716$$

Step 5

$$T = \frac{1}{\omega_{max}\sqrt{\alpha}} = \frac{1}{\frac{\omega_n}{2}\sqrt{\alpha}} = \frac{2}{0.92\sqrt{\alpha}} = 5.248$$

Giving a zero in $s = -\frac{1}{T} = -0.19$ and a pole in $s = -\frac{1}{\alpha T} = -1.11$.

Digital Controller Design Lead Compensator for Antenna - Design Example Exercises Exercises Effect of Sample Times Accommodation for Sampling Delay Effect of Sample Times

Lead Compensator Design for Antenna (FC pp. 375)

Step 6

Draw the compensated frequency response, check PM Using the formulation:

$$D(s) = \frac{Ts+1}{\alpha Ts+1}$$

we use:

```
sysD=tf([5.3 1],[0.9 1])
sysC=sys*sysD
margin(sysC)
step(feedback(sysC,1))
```



Digital Controller Design Lead Compensator for Antenna - Design Example Exercises Effect of Sampler Times Accommodation for Sampling Delay Effect of Sampling Method

Lead Compensator Design for Antenna (FC pp. 375)



Figure: Frequency response

Figure: Step response



Digital Controller Design Lead Compensator for Antenna - Design Example Exercises Effect of Sample Times Accommodation for Sampling Delay Effect of Sampling Method

Lead Compensator Design for Antenna (FC pp. 375)

Step 7

Step 7: Iterate on the design until all specifications are met

```
sysD=tf([10 1],[1 1])
sysC=sys*sysD
margin(sysC)
sysCL=feedback(sysC,1)
step(sysCL)
```



Lead Compensator Design for Antenna (FC pp. 375)



Figure: Frequency response

Figure: Step response



Digital Lead Compensator for Antenna - Fast Sampling

Continuous lead controller

$$D(s) = \frac{10s+1}{s+1}$$

Digitization - Fast Sample Rate

```
sysc=tf(1,[10 1 0]);
lead=tf([10 1],[1 1]);
syslead=sysc*lead;
Ts=1/20;
leadd1=c2d(lead,Ts,'zoh');
sysd=c2d(sysc,Ts,'zoh');
syscld=feedback(sysd*leadd1,1);
step(syscld)
```



Digital Lead Compensator for Antenna - Fast Sampling



Step Response



Digital Lead Compensator for Antenna - Slow Sampling

Continuous lead controller

$$D(s) = \frac{10s+1}{s+1}$$

Digitization - Slow Sample Rate

```
sysc=tf(1,[10 1 0]);
lead=tf([10 1],[1 1]);
syslead=sysc*lead;
Ts=1/2;
leadd1=c2d(lead,Ts,'zoh');
sysd=c2d(sysc,Ts,'zoh');
syscld=feedback(sysd*leadd1,1);
step(syscld)
```



Digital Lead Compensator for Antenna - Slow Sampling





Effect of Sample Times Accommodation for Sampling Delay Effect of Sampling Method

Effect of Sample Time on Step Response



Step Response



Effect of Sample Times Accommodation for Sampling Delay Effect of Sampling Method

Effect of Sample Time on Frequency Response









Effect of Sample Times Accommodation for Sampling Delay Effect of Sampling Method

Effect of Sample Time on Pole Locations



Pole-Zero Map



Digital Controller Design Lead Compensator for Antenna - Design Example Exercises Effect of Sample Times Accommodation for Sampling Delay Effect of Sampling Method

Incorporating Sampling Delay in System

Continuous System

$$G(s) = \frac{1}{s(10s+1)}$$

Continuous System with Delay

$$G_d(s) = rac{2/T}{s+2/T} rac{1}{s(10s+1)}$$



Lead Compensator for System using Slow Sampling Rate

Inserting T = 1/2

$$egin{aligned} G_d(s) &= rac{2/T}{s+2/T}rac{1}{s(10s+1)} \ &= rac{4}{s(s+4)(10s+1)} \end{aligned}$$



Digital Controller Design Lead Compensator for Antenna - Design Example Exercises Effect of Sample Times Accommodation for Sampling Delay Effect of Sampling Method

Lead Compensator Design for Antenna

Step 1

Design the low frequency gain ${\boldsymbol{K}}$ with respect to the steady-state error specification

Steady-state unchanged from original system: K = 1

Step 2

Determine the needed phase lead

```
sys=tf(1,[10 41 4 0]);
margin(sys)
```

PM=14 at $\omega = 0.308$



Lead Compensator Design for Antenna

Step 3

Using lead contribution of $\phi_{max}=$ 50 should result in PM=64 which is 9 more than needed.

Step 4

Determine:

$$\alpha = \frac{1 - \sin \phi_{max}}{1 + \sin \phi_{max}} = \frac{1 - \sin 50}{1 + \sin 50} = 0.1325$$

Step 5

$$T = rac{1}{\omega_{max}\sqrt{lpha}} = rac{1}{0.4\sqrt{(0.1325)}} = 6.869$$

Giving a zero in $s = -\frac{1}{T} = -0.1456$ and a pole in $s = -\frac{1}{\alpha T} = -1.099$.



Lead Compensator Design for Antenna

Step 6

Draw the compensated frequency response, check PM Using the formulation:

$$D(s) = \frac{Ts+1}{\alpha Ts+1}$$

we use:

```
sysD=tf([6.9 1],[0.9 1])
sysC=sys*sysD
margin(sysC)
step(feedback(sysC,1))
```



Digital Controller Design Lead Compensator for Antenna - Design Example Exercises Effect of Sampleing Delay Effect of Sampling Method

Lead Compensator Design for Antenna



Figure: Frequency response

Figure: Step response



Digital Controller Design Lead Compensator for Antenna - Design Example Exercises Effect of Sample Times Accommodation for Sampling Delay Effect of Sampling Method

Lead Compensator Design for Antenna

Step 7

Step 7: Iterate on the design until all specifications are met

```
sysD=tf([7.5 1],[0.68 1])
sysC=sys*sysD
margin(sysC)
sysCL=feedback(sysC,1)
step(sysCL)
```



Digital Controller Design Lead Compensator for Antenna - Design Example Exercises Effect of Sampler Times Accommodation for Sampling Delay Effect of Sampling Method

Lead Compensator Design for Antenna



Figure: Frequency response

Figure: Step response



Digital Lead Compensator for Antenna - Slow Sampling

Continuous lead controller

$$D(s) = \frac{7.5s + 1}{0.68s + 1}$$

Digitization - Slow Sample Rate

```
sysc=tf(1,[10 1 0]);
lead=tf([7.5 1],[0.68 1]);
syslead=sysc*lead;
Ts=1/2;
leadd1=c2d(lead,Ts,'zoh');
sysd=c2d(sysc,Ts,'zoh');
syscld=feedback(sysd*leadd1,1);
step(syscld)
```



Digital Controller Design Lead Compensator for Antenna - Design Example Exercises Effect of Sample Times Accommodation for Sampling Delay Effect of Sampling Method

Digital Lead Compensator for Antenna - Comparison





Figure: Frequency response

Figure: Step response



Discretization in MATLAB

Matlab

```
sysd=c2d(sys,Ts,method)
```

method:

- 'zoh': Zero order hold
- 'foh': First order hold (academic)
- 'tustin': Bilinear approximation (trapezoidal)
- 'prewarp': Tustin with a specific frequency used for prewarp
- 'matched': Matching continuous poles with discrete



Discretization of Lead Compensator - Fast Sample Rate



Figure: Frequency response

Figure: Step response



Digital Controller Design Lead Compensator for Antenna - Design Example Exercises Effect of Sampleng Delay Effect of Sampling Delay

Discretization of Lead Compensator - Fast Sample Rate



Pole-Zero Map



Discretization of Lead Compensator - Slow Sample Rate



Figure: Frequency response

Figure: Step response



Discretization of Lead Compensator - Slow Sample Rate



Pole-Zero Map



Digital Controller Design Lead Compensator for Antenna - Design Example Exercises Effect of Sample Times Accommodation for Sampling Delay Effect of Sampling Method

Some important things to remember

Discretization of compensator

Use the method suited for implementation in the system

Discrete equivalent of plant

- Use method corresponding to implementation (usually ZOH)
- Simulink can combine discrete compensator with continuous plant (digitization of plant not necessary)



Book: Digital Control

- Problem 7.4
- Problem 7.5
- Problem 7.7

